D-Flip-Flop Design: Master & Slave With Preset & Clear

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***Abstract*—Three Master/Slave D-Flip-Flop circuits are designed with preset and clear inputs, and the one with the shortest delay is created in Cadence Virtuoso. The sizing for each gate is calculated and then optimized for Cadence, where the schematics and layouts were created and simulated. Then, the full schematic is created with all of the gates, then simulated for delay measurements, followed by a snap-together standard cell layout of the full D-Flip-Flop and its simulated delays. The calculated delay, the sums of all schematic delays, the full schematic delay, the sums of all layout delays, and the snap-together delay is compared against each other.**

I. Introduction and Objectives

The purpose of a D-Flip-Flop (DFF) is to delay the changing state of the output signal Q until the rising of the clock signal. In this project, a Master-Slave DFF with a Preset & Clear is designed in Cadence Virtuoso. The design is optimized for best delay and simulated to analyze the delays. Reducing delay as much as possible is important to make the circuit operate faster for the user.

Full resolution pictures of the project can be found at my project's repository linked here: https://github.com/shahkr85/VLSI-Final-Project.

II. Background and Relevant Theory

A. D-Flip-Flop Theory

To understand how a Master-Slave DFF works, first look at the Set-Reset (SR) Flip-Flop, which can be found in Figure 1.

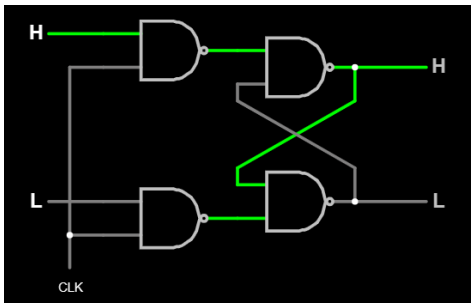

Fig. 1. SR Latch

This SR Flip-Flop utilizes a clock input. The set input (top) will set the output Q at the rising edge of clock, while the reset input (bottom) will reset the output Q to low. A D-Flip-Flop is similar to a SR Flip-Flop, as above, but difference being that both set and reset inputs are connected to a single Data input D, with the addition of an inverter in line with the reset. A Master-Slave configuration of the DFF is simply two DFFs connected to each other - the output of one connected to the input of another. Figure 2 is a positive-edge triggered, master-slave DFF, with a logic simulation at the bottom.

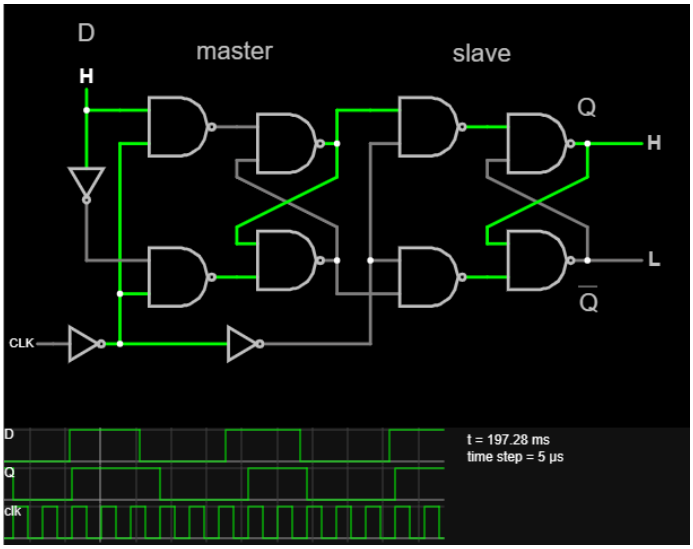

Fig. 2. Positive-Edge Triggered, Master-Slave D-Flip-Flop

This means that, when input D goes high, it will wait on the clock to go from low to high (thus the positive-edge triggered functionality) for the output to switch to high. Likewise, when input D goes low, the output will go low after a positive edge of the clock. This is verified in the logic simulation above in Figure 2. The truth table can be found below.

B. Logical Effort Calculations

When designing any logic circuit, one must calculate the delays and input capacitance for sizing each gate. To begin this process, the worst-case path must be identified, then the logical efforts, parasitic delay, and the unit capacitance of each gate must be defined.

Afterwards, the total logical effort of the circuit must be calculated. This is defined as the product of all individual logical efforts, as shown in Equation 1.

PRESET	CLEAR	DATA	CLOCK	Q	$\bar{Q}$
0	0	X	X	X	X
0	1	X	X	1	0
1	0	X	X	0	1
1	1	0	1	0	1
1	1	X	0	Q_0	$\bar{Q_0}$
1	1	0	1	1	0

TABLE I
TRUTH TABLE

Gate Type	Logical Effort	Parasitic Delay	Unit Capacitance
Inverter	1	1	1
2NOR	5/3	2	5
3NOR	7/3	3	7
2NAND	4/3	2	4
3NAND	5/3	3	5

TABLE II
GATE DEFINITIONS

$$G = \Pi g_i \tag{1}$$

Afterwards, the electrical effort must be calculated. This is derived by multiplying all of the individual electrical efforts together. Each individual electrical effort is just the load capacitance (the input capacitance of the next gate) divided by the input capacitance of the current gate. In this project, it is known that the load of the total circuit is 45C, and the driving inverter is 3C. The D-Flip-Flop has a latch at the end of the circuit, which makes one of the latching gates part of the load, which adds to the 45C. All of the electrical efforts in between the last gate and the first gate cancel out and which will simplify down to Equation 2.

$$H = \frac{45C + (LatchingGate)}{3C} \tag{2}$$

The next calculation needed is the branching effort. This is the product of all individual branching efforts. This requires identifying all of the branches in the circuit, and differentiating which ones are on the worst path and which ones are off of the path. This can be simplified to Equation 3.

$$B = \Pi b_i = \Pi(\frac{C_{on-path} + C_{off-path}}{C_{on-path}}) \tag{3}$$

The next calculation is one of the simplest, which is the parasitic delay of the whole circuit. This is the sum of all individual gate parasitic delays. Individual parasitic delay is simply equal to the number of inputs of each gate. This calculation is found in Equation

$$P = \Sigma p_i \tag{4}$$

The next calculation is the path effort, which is simply the product of the total logical effort, branching effort, and electrical effort, as shown in Equation 5.

$$F = GBH \tag{5}$$

The next calculation is called the Best Stage Effort, shown in Equation 6, with N being the number of stages in the circuit.

$$\hat{f} = \sqrt[N]{F} \tag{6}$$

The next calculation is the delay. This calculation is used to determine which design is best. This is shown in Equation 7.

$$D = N\hat{f} + P \tag{7}$$

To get this delay value in nanoseconds, use Equation 8.

$$D(ns) = \frac{D * 60}{1000} \tag{8}$$

The next calculation is the best number of stages. This number must be rounded to the next whole number, and the number of stages in the circuit should equal this number.

$$N' = \log_{3.59}(F) \tag{9}$$

Finally, the last calculation needed in this phase is the input capacitance, shown in Equation 10.

$$C_{in} = \frac{C_{out} * g_i}{\hat{f}} \tag{10}$$

This input capacitance calculation can be further simplified to Equation 11.

$$C_{in_{latch}} = \frac{C_{out} * g_i}{\hat{f} - g_i} \tag{11}$$

This input capacitance actually evaluates to a value in terms of C. In a unit inverter, the capacitance of a PMOS is 2C, while for a NMOS is 1C. The input capacitance of a gate is simply the sum of the unit NMOS and PMOS capacitances. The W/L ratio is $1.5/0.6$. To calculate C, the gate of the MOS transistor can be modeled as a parallel capacitor, in Equation 12:

$$C_g = k_{ox}\varepsilon_{ox}\frac{WL}{t_{ox}} = \varepsilon_{ox}\frac{WL}{t_{ox}} = C_{ox}WL \tag{12}$$

Here, $C_{ox}L$ will evaluate to 2fF/μm, and with a width of 1.5μm, $C = 3$fF, using the equation above.

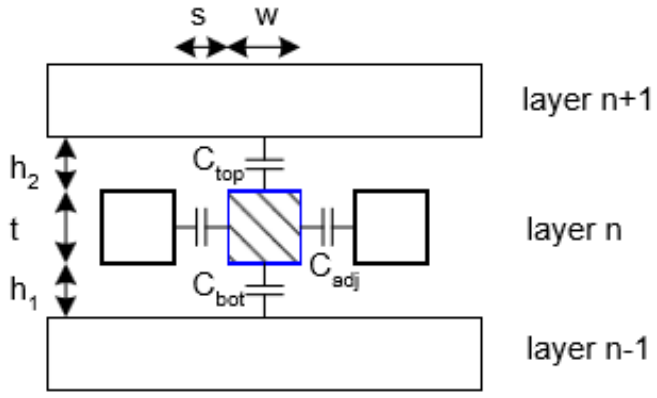

Fig. 3. Interconnect: Wire Capacitance

C. Interconnect

Another important aspect of designing logic circuits is understanding interconnect. A capacitor is any two conductors, such as metals, separated by an insulator, such as air. Wires have a capacitance per unit length, to neighboring wires and to layers above and below. The total capacitance is the sum of all individual capacitance. This is theory is shown in Figure 3.

In other words, when creating layouts in Cadence Virtuoso, it's important to avoid overlapping between metal1 and metal2 layers, and also to maximize distance between metal layers, all to minimize the parasitic capacitance. Parasitic capacitances are counterproductive in reducing the delay of the circuit, so the less the better.

Additionally, with regards to interconnect, it's important to consider wire resistance as well. The wire is split into rectangular blocks of length l and width w. Each block of wire has sheet resistance $R_{\square}$ ($\Omega/\square$). Figure 4 demonstrates how sheet resistance works.

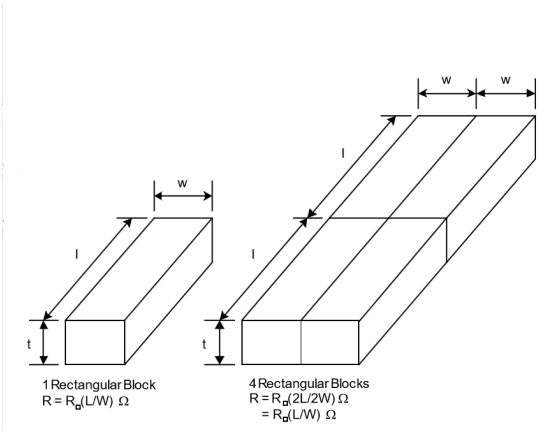

Fig. 4. Interconnect: Wire Resistance

Wire resistance is proportional to the length of the wire, as shown in Equation 13.

$$R = \frac{\rho}{t}\frac{l}{w} = R_{\square}\frac{l}{w} \tag{13}$$

This means that the longer the wires, the larger the resistance, which will increase delay.

III. Procedure

This procedure is a high-level procedure, meaning that it assumes experience working on Cadence Virtuoso with schematics, layouts and setting up simulations. This procedure is not a tutorial on Cadence.

A. Three Designs

The first phase of this project involves developing three different designs. These three designs must be a master-slave D-Flip-Flop design with a Preset and Clear inputs to the master latch. For each design, the logical effort calculations must be done on the worst paths, using Equations 1-10 from the background section above. When creating the designs, it is important for the logical truth table holds true for all designs. Otherwise, it is no longer a D-Flip-Flop. The calculations must be done until an input capacitance at the driving inverter is reached at 3C or lower. If it is lower, then it can be rounded to 3C. If the driving inverter evaluates to $C_{in} > 3$, then another iteration of calculations must be done with the new input capacitances, until $C_{in} \leq 3$ at the driving inverter.

Afterwards, it is time to select the best design. The best design is the design with the fastest delay calculation on the last iteration of input capacitance.

Additionally, the load capacitances for each gate must be calculated for the best design. To do this, at each gate, the input capacitance of the next gate must be multiplied by C = 3fF (as derived from Equation 12).

B. Size Optimization

Now it is time to do sizing optimization. First, it is important to know the unit capacitances of each gate. This is simply the unit size of the NMOS plus the PMOS of each gate. These values can be found on Table II: Gate Definitions, from the background section. First, calculate the size/gate ratio of each gate in the worst path, using Equation 14.

$$R = \frac{C_{in}}{C_{unit}} \tag{14}$$

After these ratios are calculated, it is time to calculate the new PMOS width and NMOS width in each gate. To do this, use Equations 15 & 16;

$$W_P = 1.5 * R * w_{p-unit} \tag{15}$$

$$W_N = 1.5 * R * w_{n-unit} \tag{16}$$

where w_{p-unit} and w_{n-unit} refer to the standard size of the PMOS and NMOS, respectively.

C. Folding

If folding is needed, divide the PMOS and NMOS widths by the number of parallel transistors to each input. For example, if folding a 2-input NAND once, since there are 2 of PMOS and NMOS for each input, the widths are halved. Additionally, it is important that the PMOS and NMOS size ratio match that of the same gate but of standard size. Keep in mind that all gates need to be sized appropriately, including any gates not on the worst path such as any gates on Preset & Clear.

D. Design & Simulation

Now, it is time to create the standard cell library in Cadence. Using the sizes calculated, create each individual gate with its own symbol in Cadence schematic. Each gate must be simulated for both its logic and for delay. To measure delay, the calculator can be used or it can be measured from the graph using the markers feature. Figure 5 shows how propagation delay falling (t_{pdf}) and propagation delay rising (t_{pdr}) are measured. These two measurements are then averaged for the average propagation delay (t_{apd}).

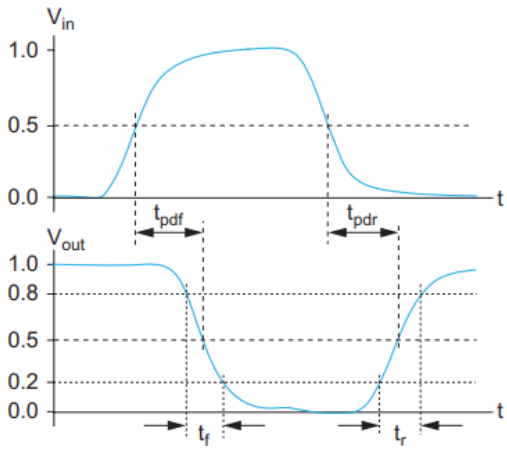

Fig. 5. Propagation Delay Measurements

After all gates are simulated, using the symbols make a new schematic with the full circuit. To simulate the full circuit, the delay must be measured from both the master and slave. From the master, measure the delay from the input D (or Data) to the output Q of the master. Then to measure the delay for the master, measure from the clock input to the slave (clock not), to the output Q of the whole circuit. These two stages of the DFF are measured independently to ensure that the pulse width is not captured in the propagation delay measurement while waiting for the slave latch to trigger. After these t_{adp} are measured, they are added together for the delay of the whole circuit.

The next step in the project is to create the layouts. For each gate, create the layouts based on the size of the PMOS and NMOS sizing as calculated earlier and they must match the sizing from the schematic. After each gate is created, a design-rule check (DRC) must pass, the layout must be extracted for parasitic capacitances, and an LVS must succeed with matching netlists (which ensures that the layout pins, nets, devices, etc. are the same as the schematic).

The next step is to create the full, snap-together, standard cell layout. In standard cell design, all cells have a fixed height. That means to space out all NMOS and PMOS to the maximum height of the cell. The maximum height of each cell is as big as the biggest gate, which tends to be the last gate, so the cell may have a triangular-type shape since the sizing of each device gets larger the further along the path of the circuit. Additionally, in standard cell design, wiring is restricted to channels. That means all of the connections must be made on a set of rails. The number of rails needed is equal to the number of nets in the full schematic. Figure 6 demonstrates what the standard cell design looks like.

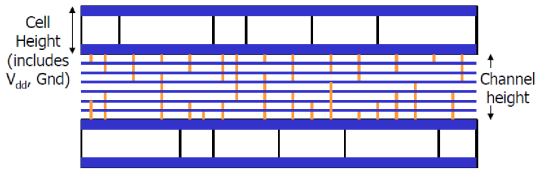

Fig. 6. Standard Cell Design

After this is completed, this snap-together layout can be checked with DRC, extracted for parasitic capacitances, and succeeded an LVS process, and then simulated again in the same way as was done with the full schematic.

Now, the final step is to compare all of the delays. Make sure all individual gates from both the schematic and layout have delay measurements, and sum all of those delays. Compare the layout delay and schematic delay, as well as the delay from mathematical calculations.

IV. Results and Discussion

A. Design 1

The first design that was created had a worst path as follows:

INV-INV-NAND2-NAND3-NAND2-NAND2

This design was tested for correct logic using the Falstad simulator. This design can be found in Figure 7. This design has a total of 6 stages. The line in red is the worst path in the circuit.

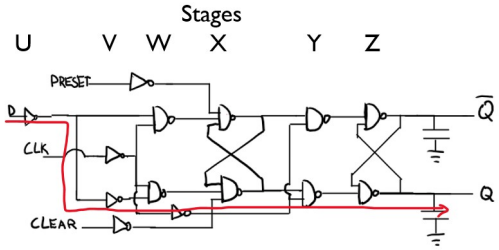

Fig. 7. Design 1

The logical effort calculations can be found in Table III. These numbers were calculated using the equations from the background. There were a total of two iterations after sizing to get to a C_{in} of 3C at the driving inverter. There are two branches, at stages X and U, with the last latch being part of the load instead of a branch.

Calculation	Iteration 1	Iteration 2
Logical Effort, G	3.950617284	3.950617284
Electrical Effort, H	16.33333333	30.30285309
Branching Effort, B	5.25	9.871846616
Parasitic Delay, P	11	11
Path Effort, F	338.7654321	1181.807872
Best Stage Effort, $\hat{f}$	2.640279161	3.251555314
Best Number of Stages, N'	4.557601134	5.535178539
Delay, D	26.84167497	30.50933188
Delay, ns	1.610500498	1.830559913

TABLE III
DESIGN 1: LOGICAL EFFORT CALCULATIONS

The input capacitances of each gate used for sizing can be found in Table VI, at each stage, where stage Z is the very last stage. If any gate is calculated to a value below 3C, it is rounded up to 3C.

Stage	Input Capacitance (C): Iteration 1	Input Capacitance (C): Iteration 2
Z	45.90855926	31.27896594
Y	23.18368953	12.82625817
X	39.68671597	13.48807501
W	20.04167668	5.530922365
V	7.59074153	3
U	10.4657184	3

TABLE IV
DESIGN 1: INPUT CAPACITANCE

B. Design 2

The next design involves changing all of the NAND gates to NOR gates. This design has a worst path as follows:

INV-INV-NOR2-NOR3-NOR2-NOR2

This design also has 6 stages. This design can be found in Figure 8, and the logic was tested for correctness using the Falstad simulator. The line in red indicates the worst path.

The logical effort calculations can be found in Table VII. These numbers were calculated using the Equations 1-9. There were a total of two iterations in this design as well, after sizing to get to a C_{in} of 3C at the driving inverter. This table shows

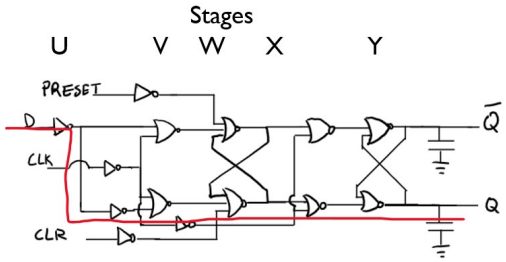

Fig. 8. Design 2

that the delay of this design is much larger than Design 1, and may not be used.

Calculation	Iteration 1	Iteration 2
Logical Effort, G	10.80246914	10.80246914
Electrical Effort, H	16.66666667	30.91143055
Branching Effort, B	6.4	15.16988474
Parasitic Delay, P	11	11
Path Effort, F	1152.26337	5065.52449
Best Stage Effort, $\hat{f}$	3.237864173	4.14416848
Best Number of Stages, N'	5.515370881	6.673863212
Delay, D	30.42718504	35.86501088
Delay, ns	1.8256311	2.1519007

TABLE V
DESIGN 2: LOGICAL EFFORT CALCULATIONS

The input capacitances of each gate used for sizing can be found in Table VI, at each stage, where stage Z is the very last stage. If any gate is calculated to a value below 3C, it is rounded up to 3C.

Stage	Input Capacitance (C): Iteration 1	Input Capacitance (C): Iteration 2
Z	47.73429	30.27243
Y	24.57087	12.17471
X	63.38318	15.6876
W	32.62602	6.309106
V	10.0764	3
U	13.18845	3

TABLE VI
DESIGN 2: INPUT CAPACITANCE

C. Design 3

The next design involves making the master portion of the D-Flip-Flop all NORs and the slave portion all NANDs. This design has a worst path as follows:

INV-INV-NOR2-NOR3-NAND2-NAND2

This design also has 6 stages, and it can be found in Figure 9, and the logic was tested for correctness using the Falstad simulator. The line in red indicates the worst path.

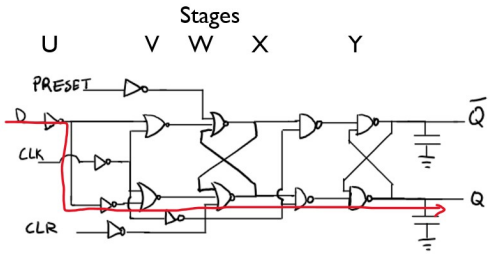

Fig. 9. Design 3

The logical effort calculations for Design 3 can be found in Table VII. These numbers were calculated using the Equations 1-9. There were a total of two iterations in this design as well, after sizing to get to a C_{in} of 3C at the driving inverter. This table shows that the delay of this design after a second iteration is also much larger than Design 1.

Calculation	Iteration 1	Iteration 2
Logical Effort, G	6.913580247	6.913580247
Electrical Effort, H	16.33333333	26.55351874
Branching Effort, B	7.333333333	17.03657376
Parasitic Delay, P	11	11
Path Effort, F	828.093278	3127.57221
Best Stage Effort, $\hat{f}$	3.064407688	3.824146819
Best Number of Stages, N'	5.25690586	6.296599353
Delay, D	29.38644613	33.94488091
Delay, ns	1.7631868	2.0366929

TABLE VII
DESIGN 3: LOGICAL EFFORT CALCULATIONS

The input capacitances of each gate used for sizing can be found in Table VIII, at each stage, where stage Z is the very last stage. If any gate is calculated to a value below 3C, it is rounded up to 3C.

See Table IX for design comparison against their delays. From this table, it is clear the Design 1 has the best delay, so it will be used in Cadence Virtuoso.

D. Size Optimization

Now it is time to begin the sizing optimization. Using the equations from Section III-B: Size Optimizations, the PMOS & NMOS widths are calculated. It is from here when the decision whether to fold or not is made. As a designer's decision, I chose to fold only once when either PMOS or NMOS width exceeds 12μm. This means that gates from stages Z and X were folded, evident in Table X below.

Stage	Input Capacitance (C): Iteration 1	Input Capacitance (C): Iteration 2
Z	34.66056	24.08852
Y	15.08092	8.398742
X	48.133	13.14521
W	26.17852	5.72904
V	8.542768	3
U	11.33051	3

TABLE VIII
DESIGN 3: INPUT CAPACITANCE

Design	Delay D	Delay (ns)
1	30.50933188	1.830559913
2	35.86501088	2.151900653
3	33.94488091	2.036692855

TABLE IX
DESIGN COMPARISON

Stage	Gate Ratio	PMOS Width (μm)	NMOS Width (μm)	PMOS Width (μm), Rounded, After Folding	NMOS Width (μm), Rounded, After Folding
Z	7.8197415	23.459224	23.459224	11.7	11.7
Y	3.2065645	9.6196936	9.6196936	9.6	9.6
X	2.6976150	8.0928450	12.139268	4	6
W	1.3827306	4.1481918	4.1481918	4.2	4.2
V	1	3	1.5	3	1.5
U	1	3	1.5	3	1.5

TABLE X
SIZE OPTIMIZATION

Additionally, in this design, there are inverters not on the worst path that must be sized appropriately. These inverters are labeled as the Master Clock, Slave Clock, Preset, and Clear. These sizes are found in Table XI.

E. Schematic Design & Simulation

Now the next step was to create the schematics of each gate. Refer to Appendix A, Figures 18 to 26 are the schematics of all of the gates, sized appropriately based on Tables X & XI. The load capacitance was calculated by substituting C = 3fF (as derived earlier in the background). These load values can be found in Table below, and are used for the layout simulations as well. These load capacitances account for branching at stages X and U.

Additionally, both the schematic gates and layout gates are simulated in a similar fashion. A block/symbol of each gate/full circuit is brought into a new schematic file and loaded based on the table above. To see how each simulation is set

Inverter	Gate Ratio	PMOS Width (μm)	NMOS Width (μm)	PMOS Width (μm), Rounded, After Folding	NMOS Width (μm), Rounded, After Folding
Master CLK	1.9427780	5.8283342	2.9141671	6	3
Slave CLK	2.629769	7.889306	3.944653	7.8	7.8
PRESET	1.3827306	4.1481918	2.0740959	4.2	2.1
CLEAR	1.3827306	4.1481918	2.0740959	4.2	2.1

TABLE XI
NON-PATH INVERTER SIZING

Stage/Gate	Load Capacitance (fF)
Z	228.8368978
Y	93.83689782
X	78.94299954
W	40.46422502
V	16.5927671
U	25.5927671

TABLE XII
LOAD CAPACITANCE

up, refer to Appendix B to see both schematic and layout simulations are set up.

The gate simulation curves can all be found in Appendix D, however, the delay measurements can be found below in Table XIII. The Netlists for this can be found in Appendix H, including the full schematic.

Stage	Fall Time (ps)	Rise Time (ps)	Prop. Delay Falling (ps)	Prop. Delay Rising (ps)	Average Prop. Delay (ps)
Z	209.9	270.5	160	209.5	184.75
Y	212.5	272.6	162.1	212.1	187.1
X	272.9	93.05	262.7	95.07	178.885
W	230.2	292.9	177	227.8	202.4
V	180.6	138.8	169.2	118.1	143.65
U	249.1	191.9	219	152.3	185.65
Sum					1082.485

TABLE XIII
SCHEMATIC DELAY SIMULATIONS

After this was completed, the full schematic was created with every symbol of each individual gate. All of the gate symbols can be found in Appendix C. This full schematic can be found in Figure 10 below.

Additionally, refer to Figure 11 below for a Cadence simulation demonstrating the logical functionality of this D-Flip-Flop. The first signal is the DATA input, the second signal is CLOCK input, the third signal is the Q output, and the fourth signal is the $\bar{Q}$ output.

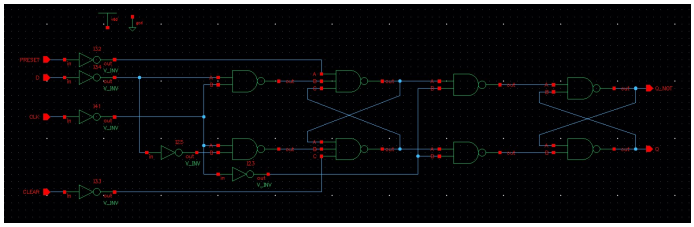

Fig. 10. Full Circuit Schematic

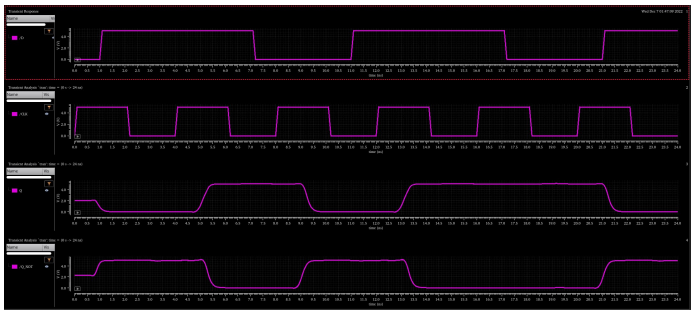

Fig. 11. Full Circuit Logic

This simulation shows that when DATA goes high, the output will wait for a rising CLOCK edge for the output Q to switch, and as a result $\bar{Q}$ is inverted. This shows that the full schematic works properly. This simulation above is where PRESET & CLEAR are both pulled low (thus going through PRESET and CLEAR inverters forcing them high, and allowing it to follow the truth table). Additionally, Figure 12 shows it working with PRESET changing (first signal, then DATA, CLOCK, Q, and $\bar{Q}$). When preset goes low (or high after its inverter) the circuit finally starts working as usual, but before that logic switch, the output will not change regardless of DATA.

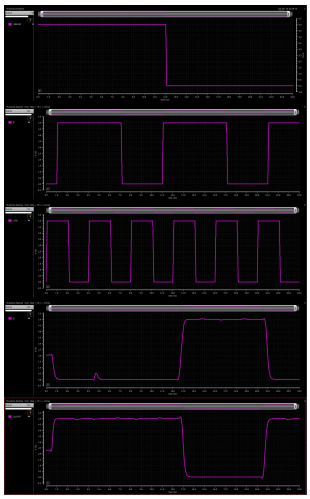

Fig. 12. Full Circuit Logic With Changing PRESET

Finally, when measuring the delays, both the master and slave delay was measured. For master delay measurements, it was from the DATA signal to the output Q signal of the master, and for slave delay measurements, it was from the CLOCK inverter signal, to the output Q of the slave. Refer to Figures 13 and 14 below for the MASTER & SLAVE simulation results, respectively.

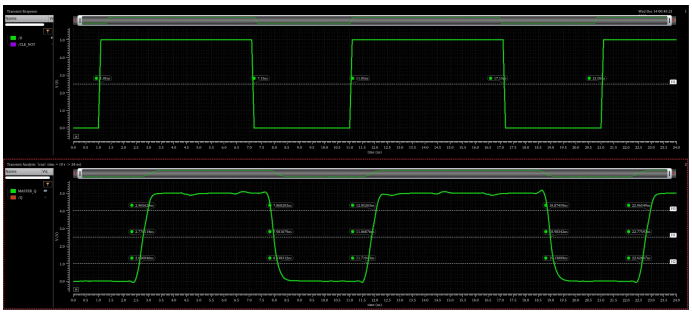

Fig. 13. Master Schematic Results

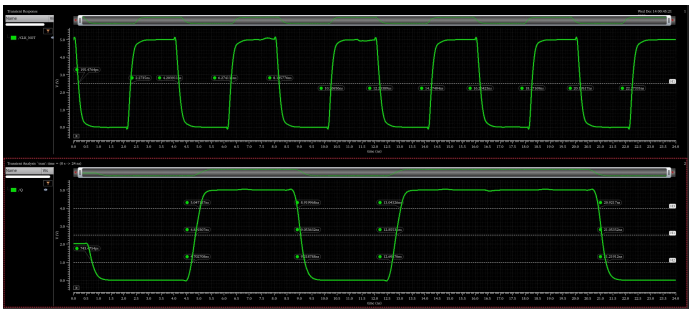

Fig. 14. Slave Schematic Results

Additionally, refer to Table XIV for MASTER, SLAVE, and the total delay. The total delay is close to the calculations.

	Prop. Delay Falling (ns)	**Prop. Delay Rising (ns)**	**Average Prop. Delay (ns)**
Master	0.8319	1.726	1.27895
Slave	0.8579	0.6554	0.75665
Total			2.0356

TABLE XIV
FULL SCHEMATIC DELAY

F. Layout Design & Simulation

The layouts of each gate needed to be completed with simulations. Refer to Appendix E: Individual Gate Layouts for figures of all gate layouts. Additionally, refer to Appendix F for all of the individual layouts extracted. These layouts also succeeded with LVS, and the simulations curves can be found in Appendix G. Refer to Table XV below for all delay measurements from the individual layout simulations. Refer to Appendix I for all Netlists of the layouts, including the snap-together layout.

Stage	**Fall Time (ps)**	**Rise Time (ps)**	**Prop. Delay Falling (ps)**	**Prop. Delay Rising (ps)**	**Average Prop. Delay (ps)**
Z	179.4	187	151.3	157	154.15
Y	186.4	193	153.8	165	159.4
X	222.9	78.42	212.7	86.91	149.805
W	206.1	210.9	171.1	177.5	174.3
V	180.4	138.7	168.7	118.1	143.4
U	249	191.7	218.5	152.2	185.35
Sum					966.405

TABLE XV
LAYOUT DELAYS

After this was completed, the next step was to create a full, snap-together layout of the whole D-Flip-Flop. This involved utilizing a lot of the interconnect theory from the background section. Figure 15 shows the full layout of the D-Flip-Flop schematic. The extracted layout can be found in Appendix F, Figure 61.

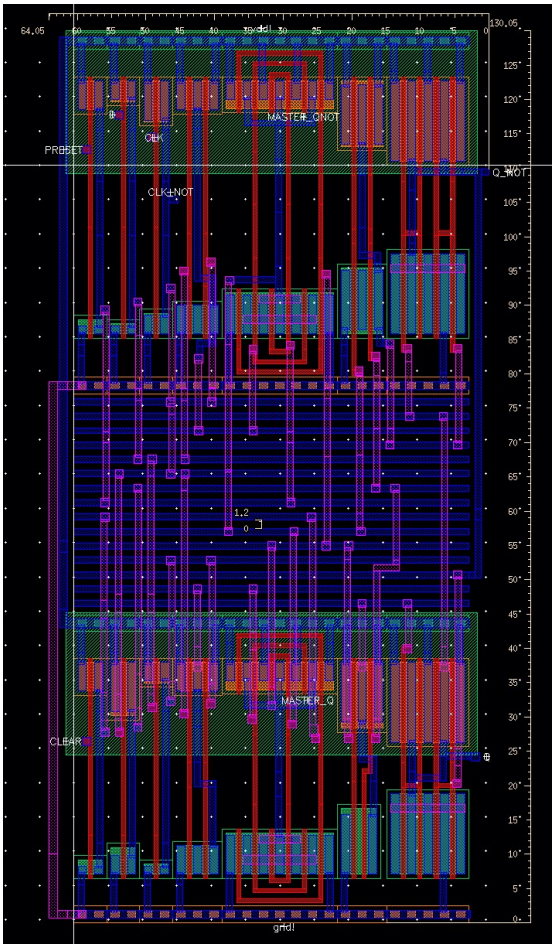

Fig. 15. Full Circuit Layout

The MASTER simulation from the layout can be found in

Figure 16.

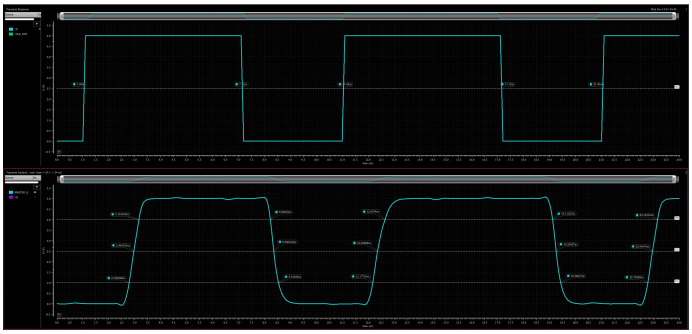

Fig. 16. Full Layout: MASTER Simulation

The SLAVE simulation from the layout can be found in Figure 17.

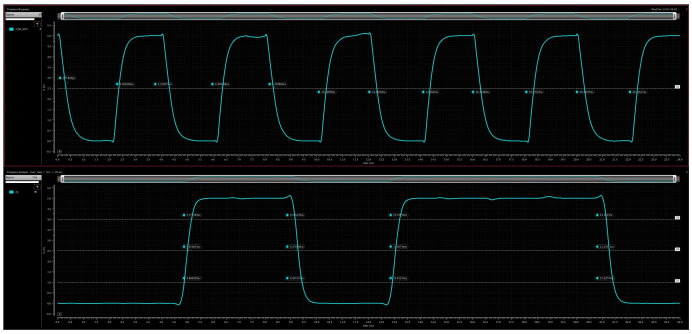

Fig. 17. Full Layout: SLAVE Simulation

Together, Table XVI shows the delays of the MASTER, SLAVE, and the total delay of the circuit.

	Prop. Delay Falling (ns)	**Prop. Delay Rising (ns)**	**Average Prop. Delay (ns)**
Master	1.21	1.915	1.5625
Slave	0.9569	0.6959	0.8264
Total			2.3889

TABLE XVI
FULL LAYOUT DELAY

Refer to Appendix J for all Layout Versus Schematic (LVS) checks.

Now it's time to compare all of the delays. Refer to Table XVII for all delays gathered for this project. Both the full schematic and snap-together layout delays are close to the calculated delay. The snap-together layout has a slightly high delay due to parasitic capacitances; there are various factors such as wire capacitance and wire resistance, as mentioned earlier in the background. There are occasionally overlapping metal1 and metal2 layers, which was unavoidable. Additionally, the nature of standard cell layout forces lengthy wires since they are connected through channels, instead of through the cells themselves, which adds to the delay. Additionally, the summed delays from the schematic and layout gates are very low compared to the full schematic and layouts because there are rounding capacitive values per gate. The whole schematic/layout does not round.

Source	**Propagation Delay (ns)**
Calculation	1.830559913
Schematic Sums	1.082435
Full Schematic	2.0356
Layout Sums	0.966405
Snap-Together Layout	2.3889

TABLE XVII
DELAY COMPARISON

V. CONCLUSIONS

Initially, three designs were created and they were calculated for best delay. The design with the best delay was selected to design in Cadence.

A fully functioning D-Flip-Flop was created in Cadence Virtuoso using various VLSI concepts. The delays of the schematic and layout were very similar, but the snap-together layout had a larger delay due to wire resistance and capacitance.

REFERENCES

[1] E., W. N. H., &; Harris, D. M. (2015). Chapter 2: MOS Transistor Theory. In CMOS VLSI Design: A circuits and systems perspective (Fourth). essay, Pearson.

[2] "Falstad Circuit Simulator," Circuit simulator applet. [Online]. Available: https://www.falstad.com/circuit/. [Accessed: 21-Dec-2022].

APPENDIX A
INDIVIDUAL GATE SCHEMATICS

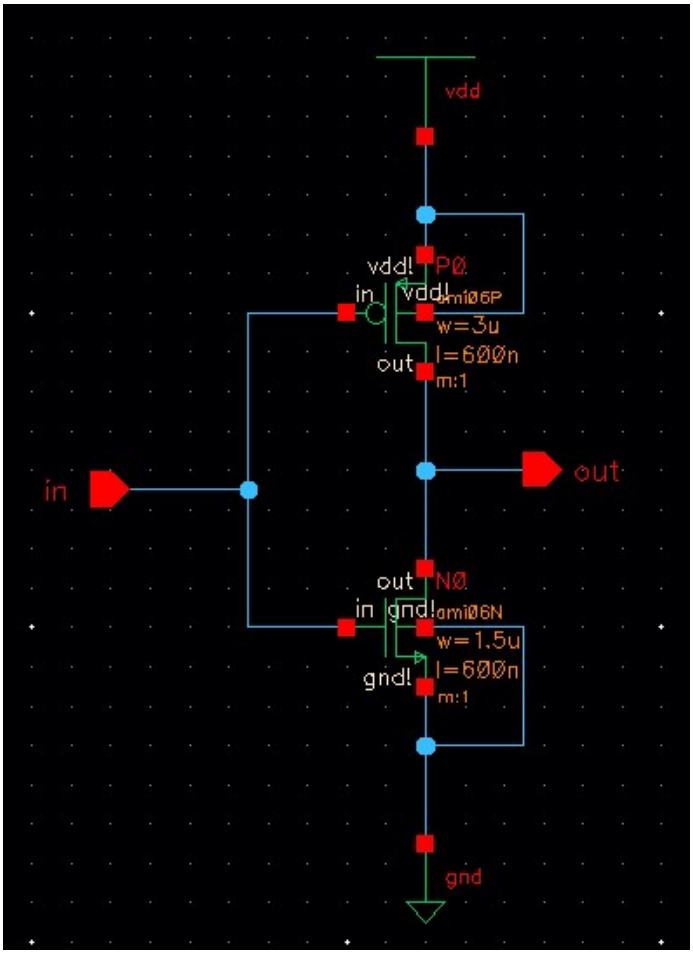

Fig. 18. Stage U: Inverter, Schematic

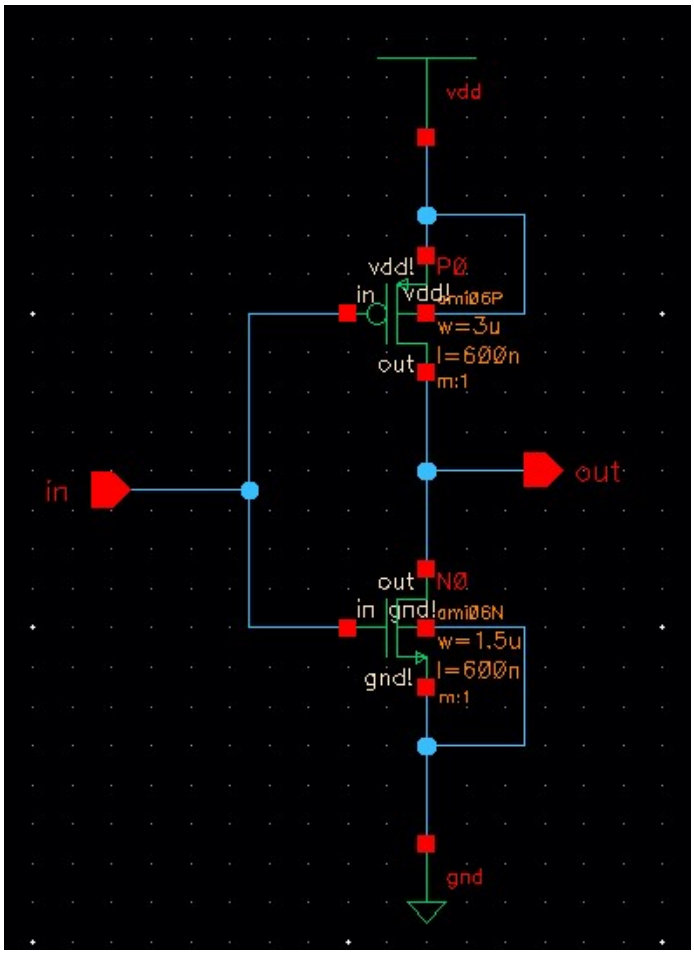

Fig. 19. Stage V: Inverter, Schematic

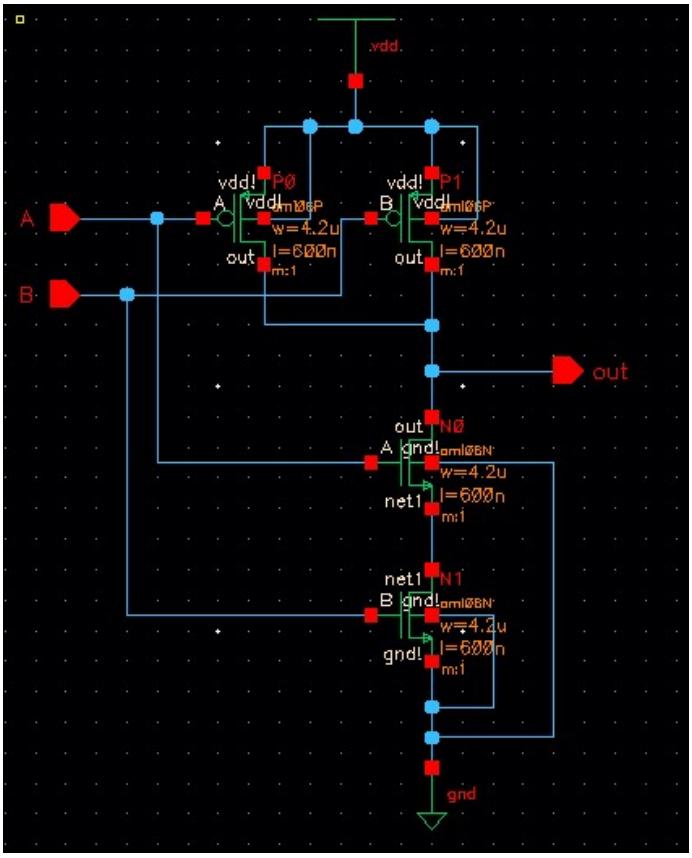

Fig. 20. Stage W: NAND2, Schematic

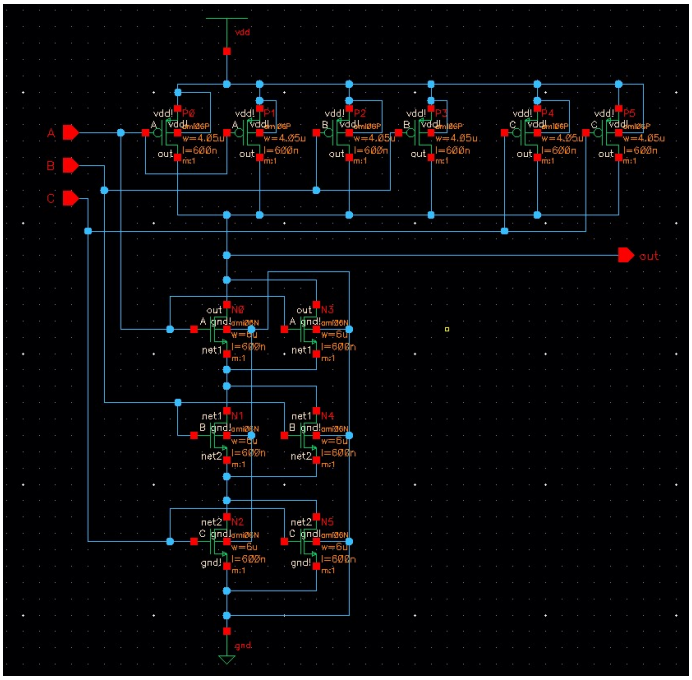

Fig. 21. Stage X: NAND3, Schematic, Folded Once

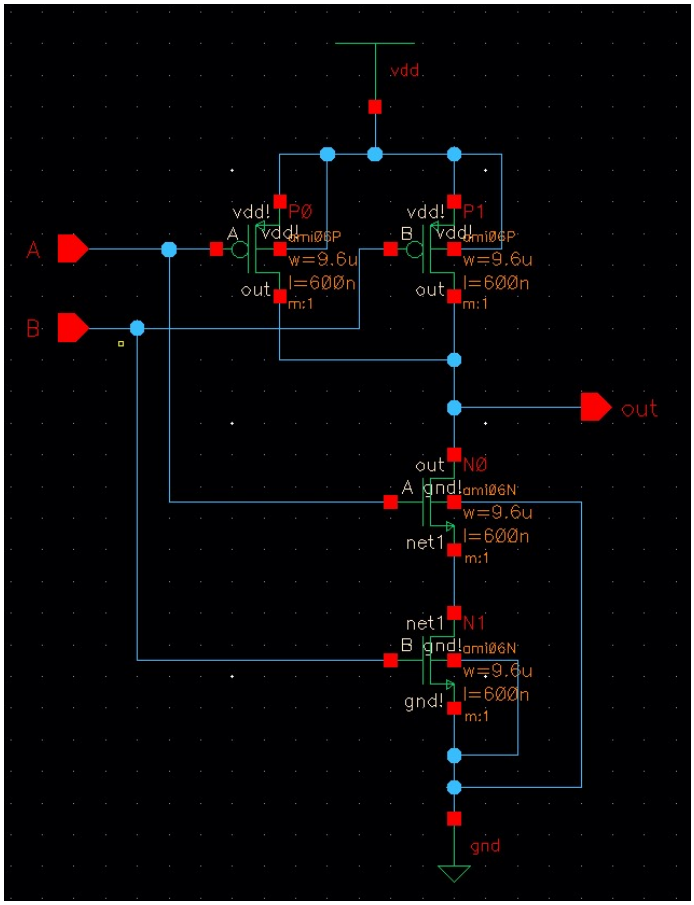

Fig. 22. Stage Y: NAND2, Schematic

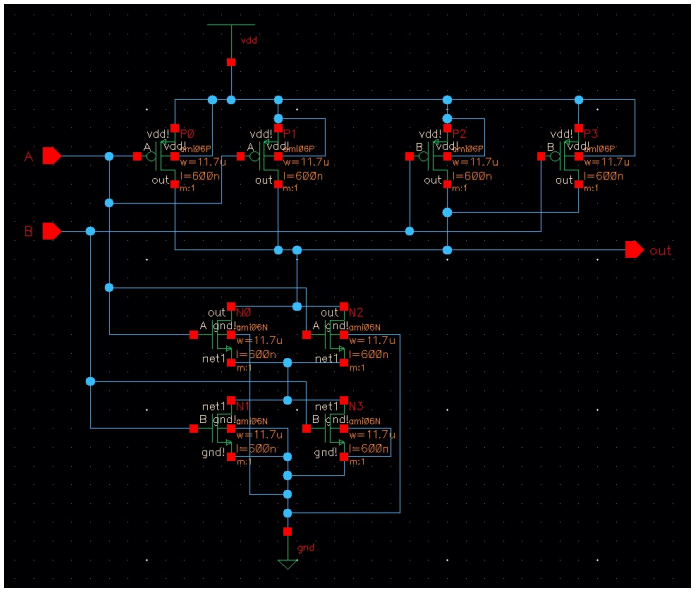

Fig. 23. Stage Z: NAND2, Schematic, Folded Once

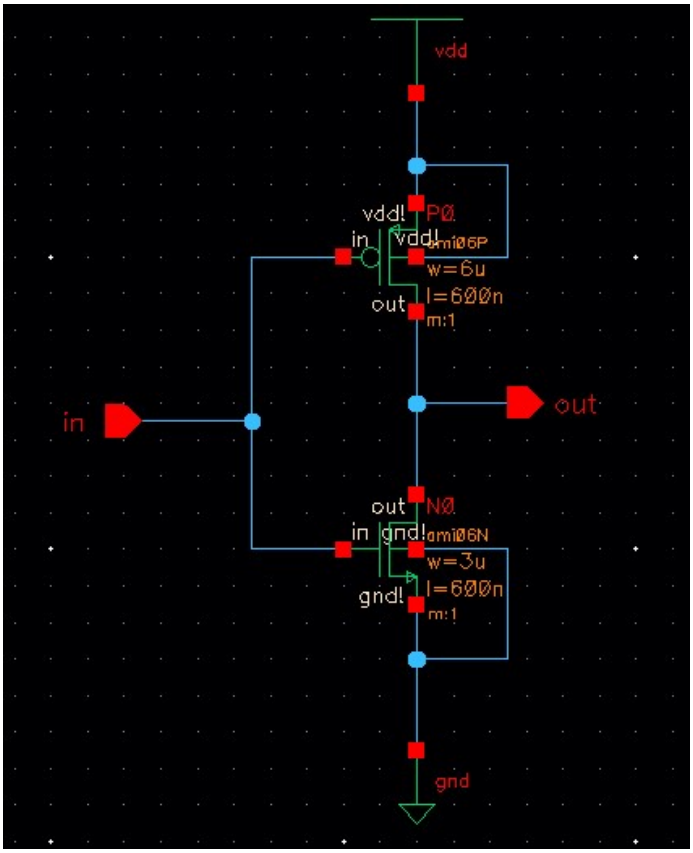

Fig. 24. Master Clock: Schematic

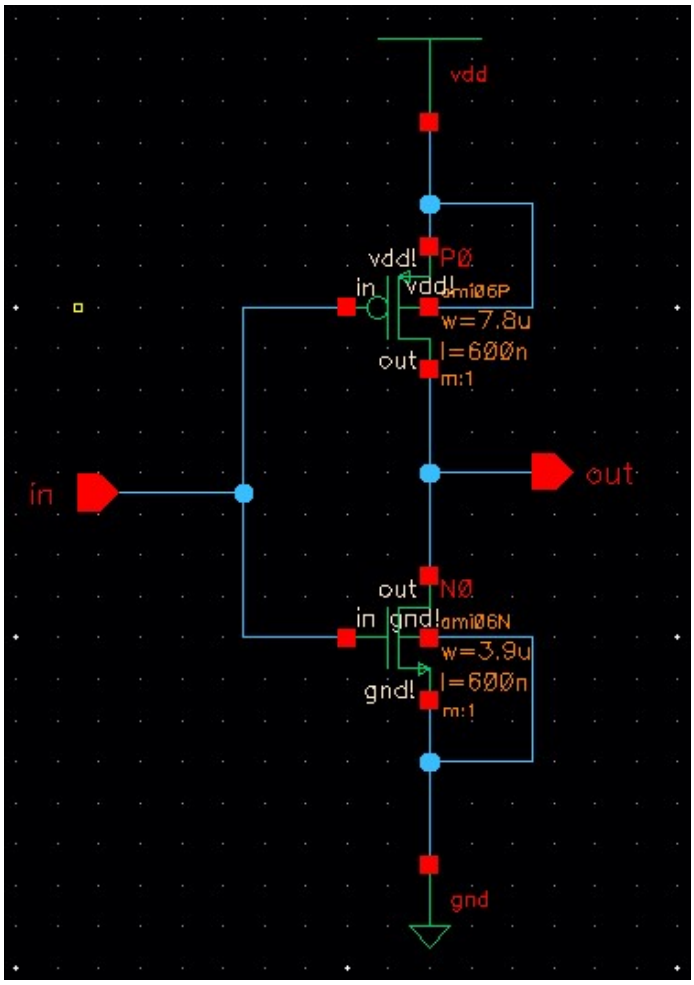

Fig. 25. Slave Clock: Schematic

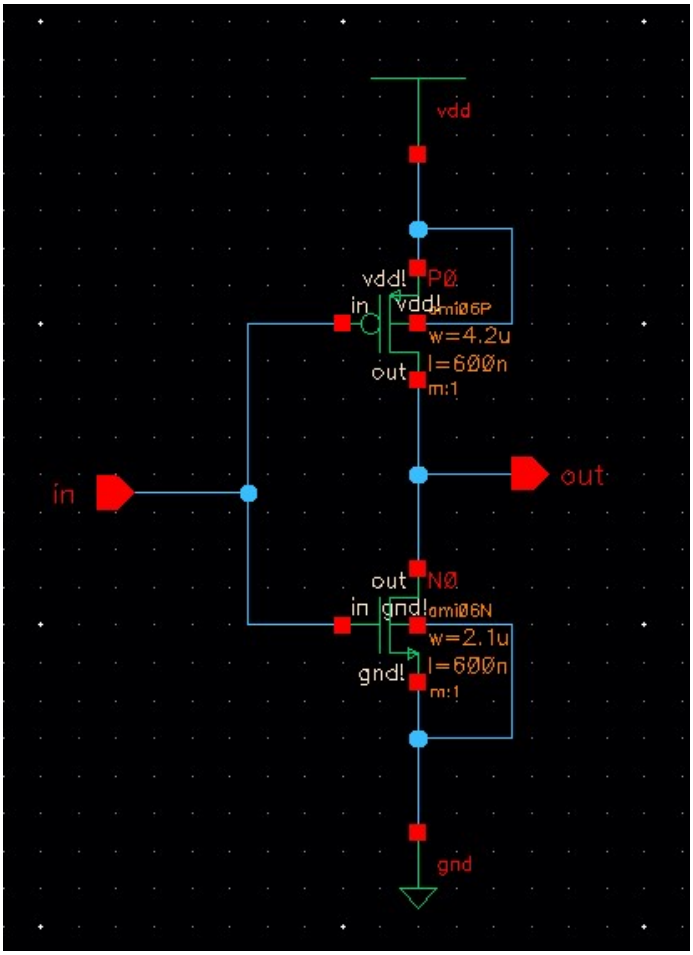

Fig. 26. Preset & Clear: Schematic

APPENDIX B
SIMULATION SETUP SCHEMATICS

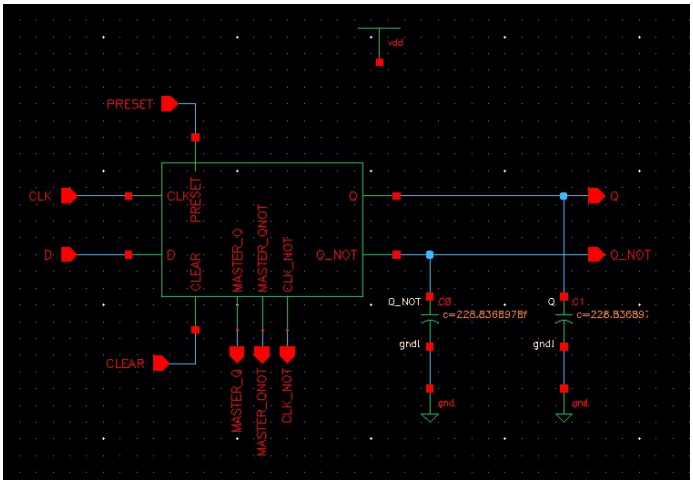

Fig. 27. Full Circuit, Simulation Schematic

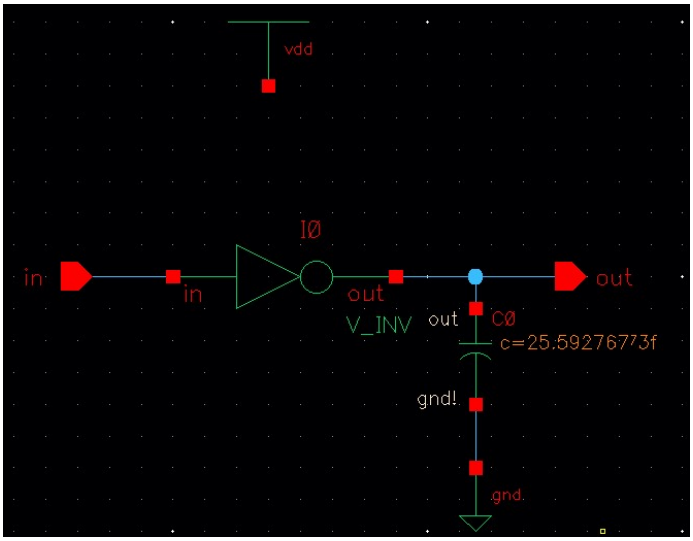

Fig. 28. Stage U: Inverter, Simulation Schematic

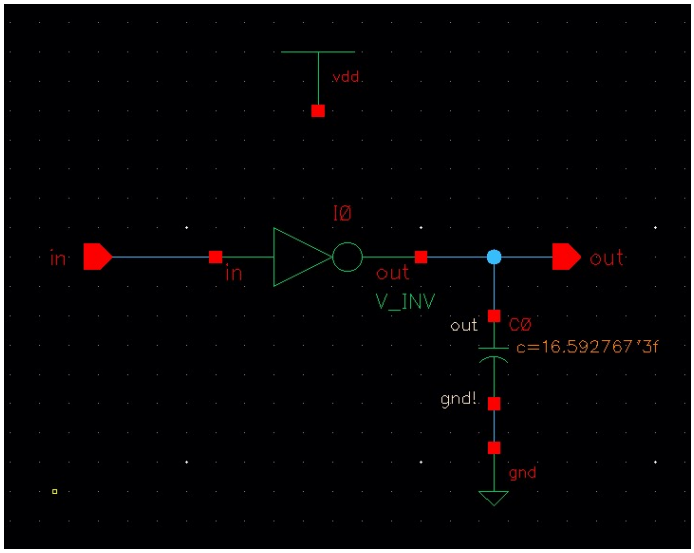

Fig. 29. Stage V: Inverter, Simulation Schematic

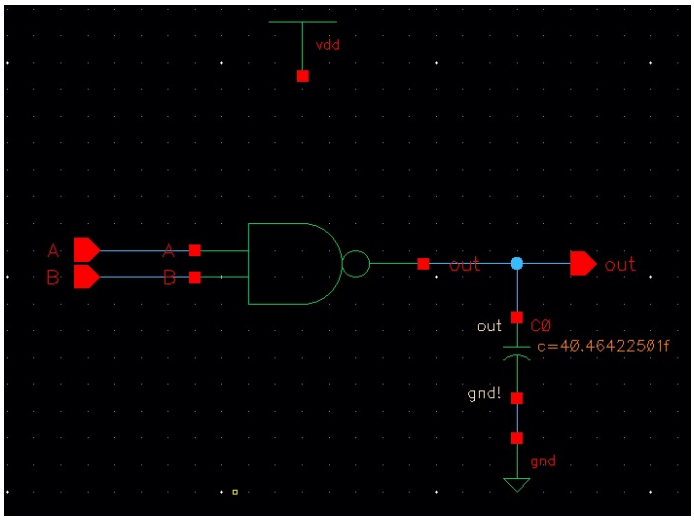

Fig. 30. Stage W: NAND2, Simulation Schematic

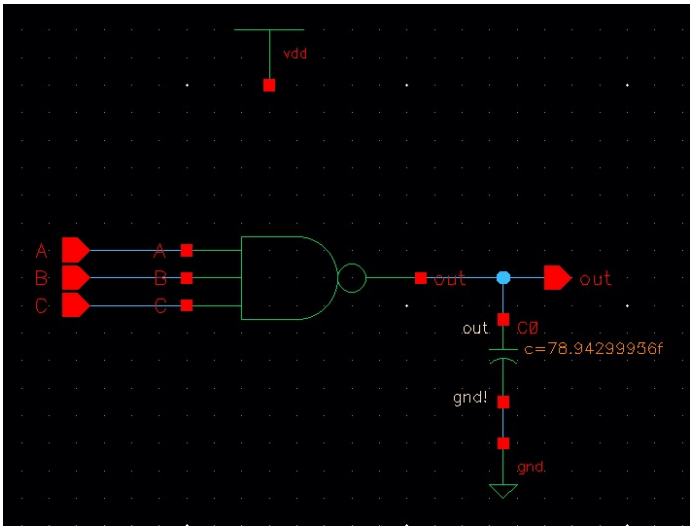

Fig. 31. Stage X: NAND3, Simulation Schematic

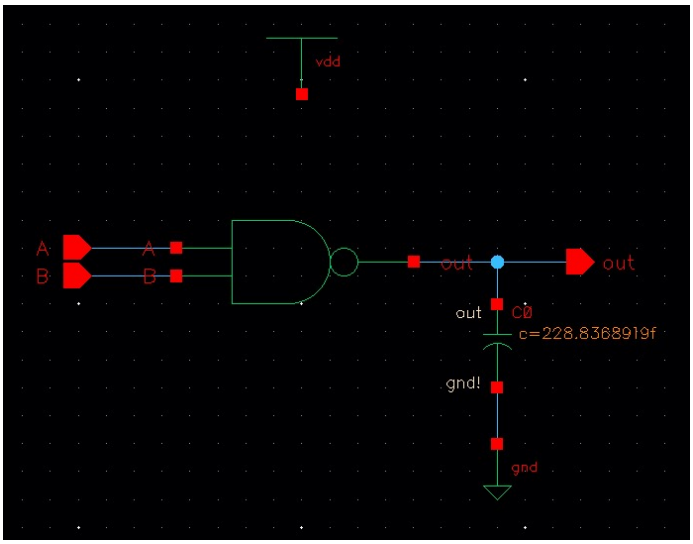

Fig. 33. Stage Z: NAND2, Simulation Schematic

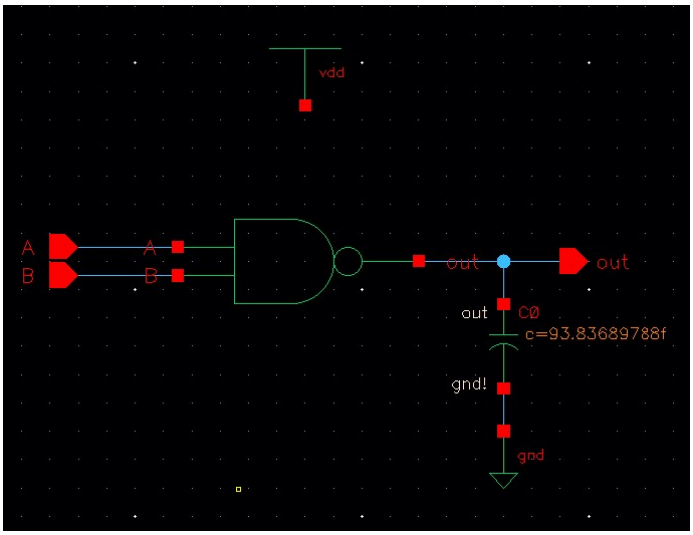

Fig. 32. Stage Y: NAND2, Simulation Schematic

APPENDIX C
INDIVIDUAL GATE SYMBOLS

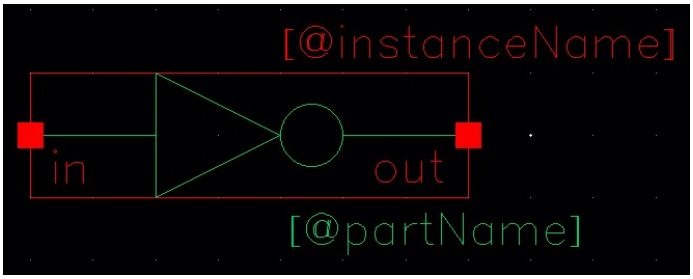

Fig. 34. Inverter Symbol

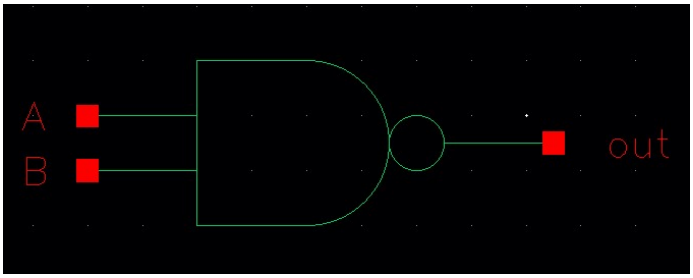

Fig. 35. NAND2 Symbol

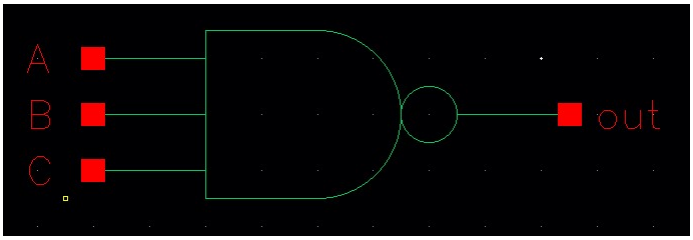

Fig. 36. NAND3 Symbol

APPENDIX D
SCHEMATIC GATE SIMULATIONS

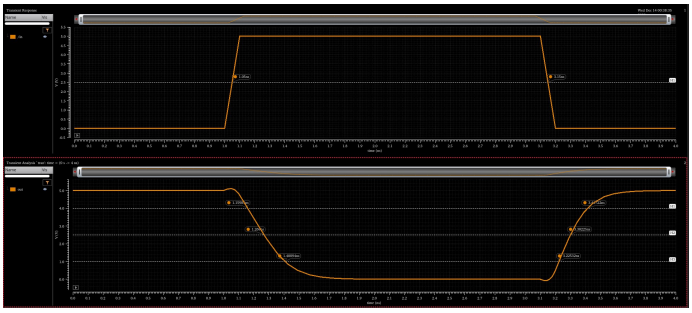

Fig. 37. Stage U: Inverter, Schematic Simulation

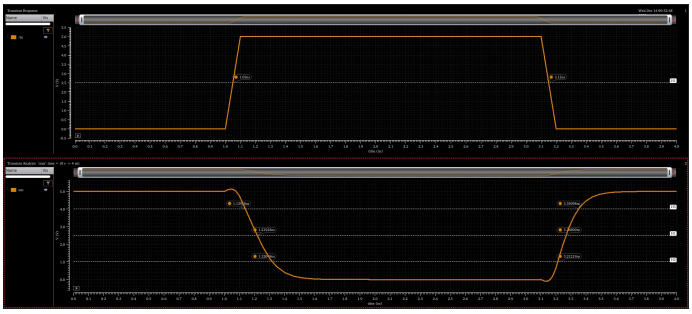

Fig. 38. Stage V: Inverter, Schematic Simulation

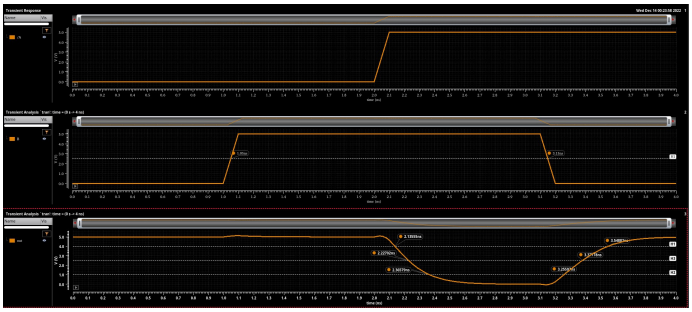

Fig. 39. Stage W: NAND2, Schematic Simulation

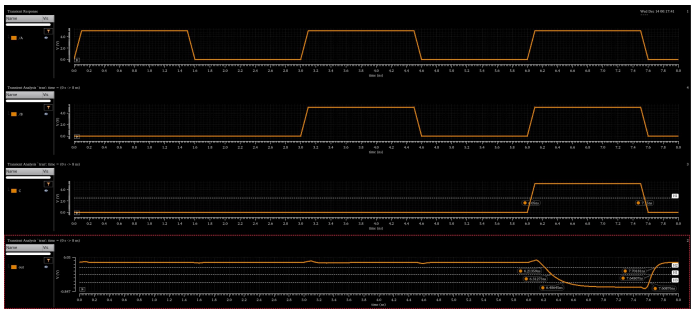

Fig. 40. Stage X: NAND3, Schematic Simulation

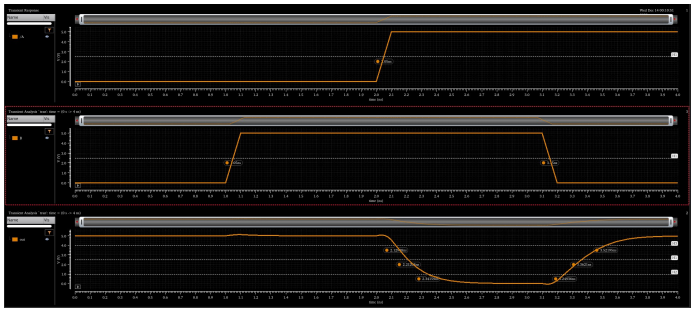

Fig. 41. Stage Y: NAND2, Schematic Simulation

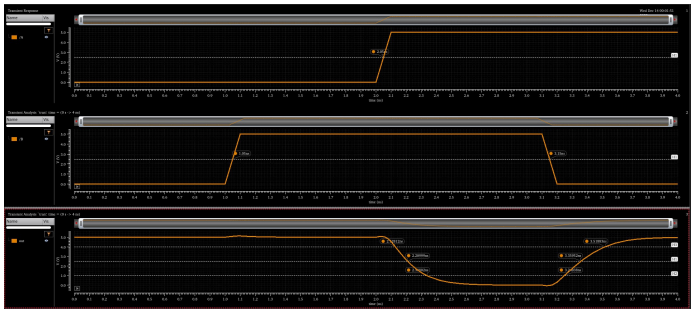

Fig. 42. Stage Z: NAND2, Schematic Simulation

APPENDIX E
INDIVIDUAL GATE LAYOUTS

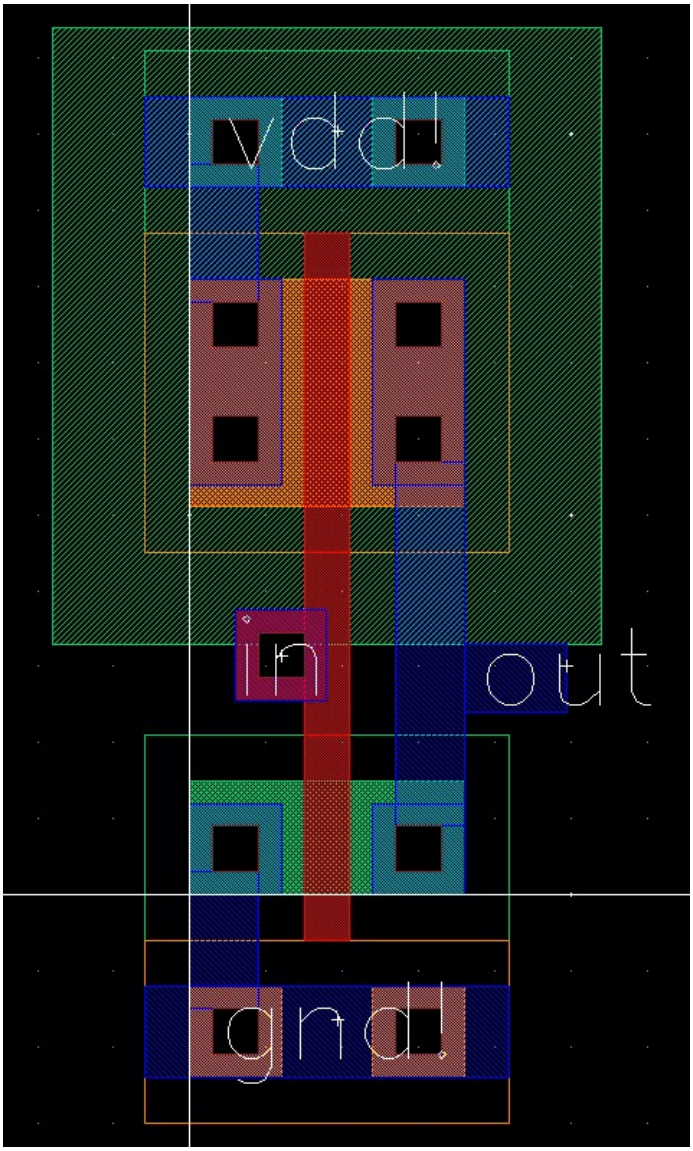

Fig. 43. Stage U: Inverter, Layout

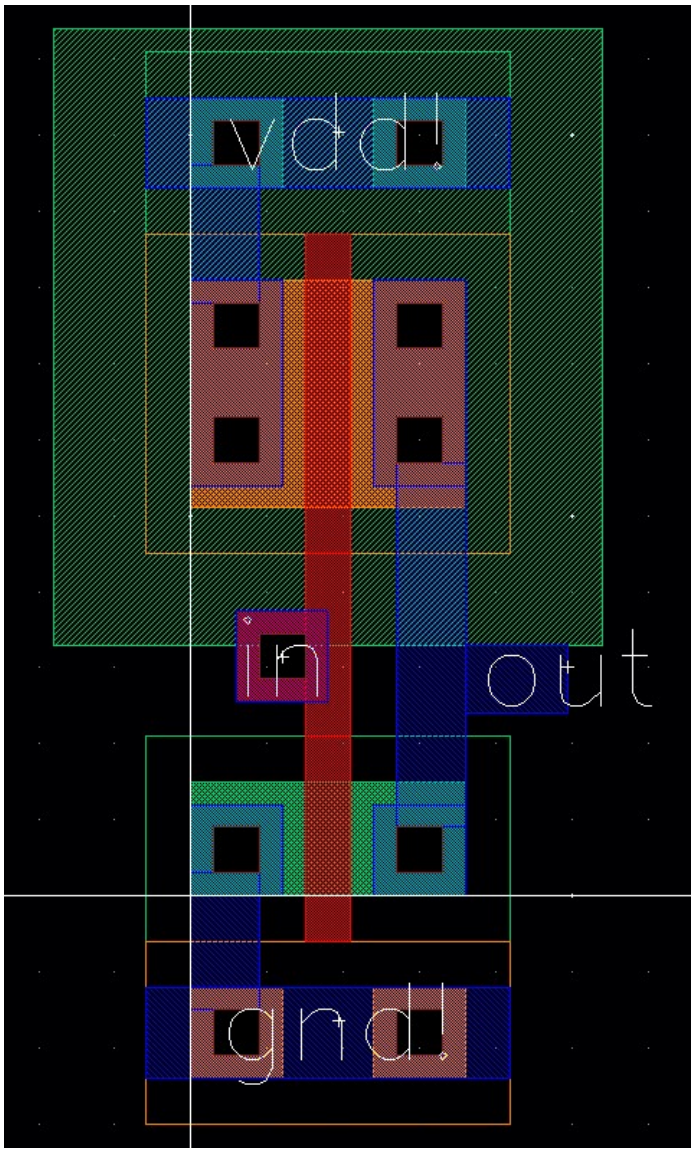

Fig. 44. Stage V: Inverter, Layout

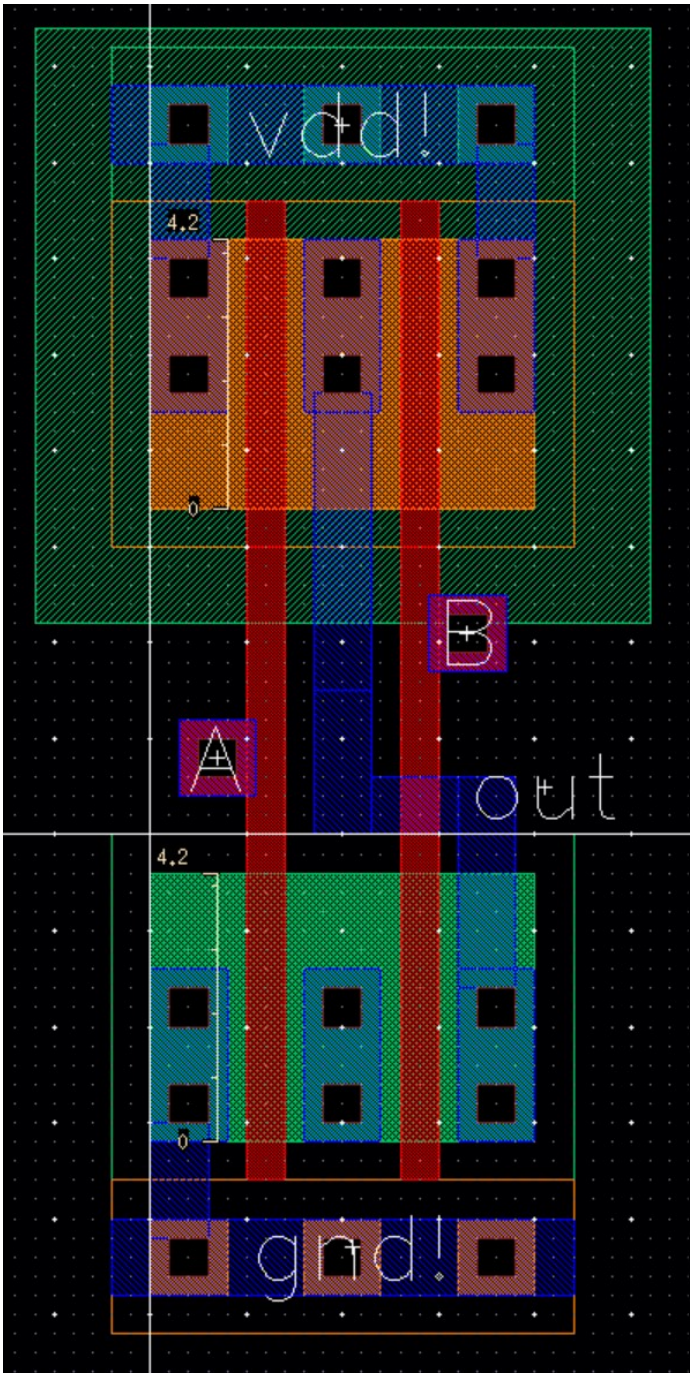

Fig. 45. Stage W: NAND2, Layout

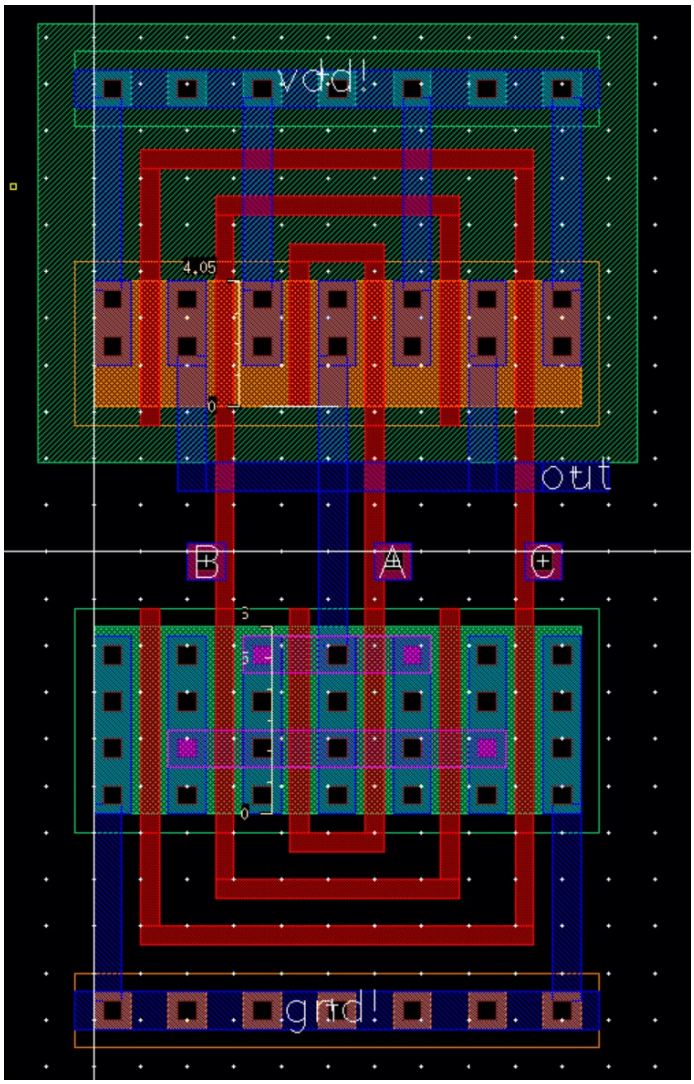

Fig. 46. Stage X: NAND3, Layout

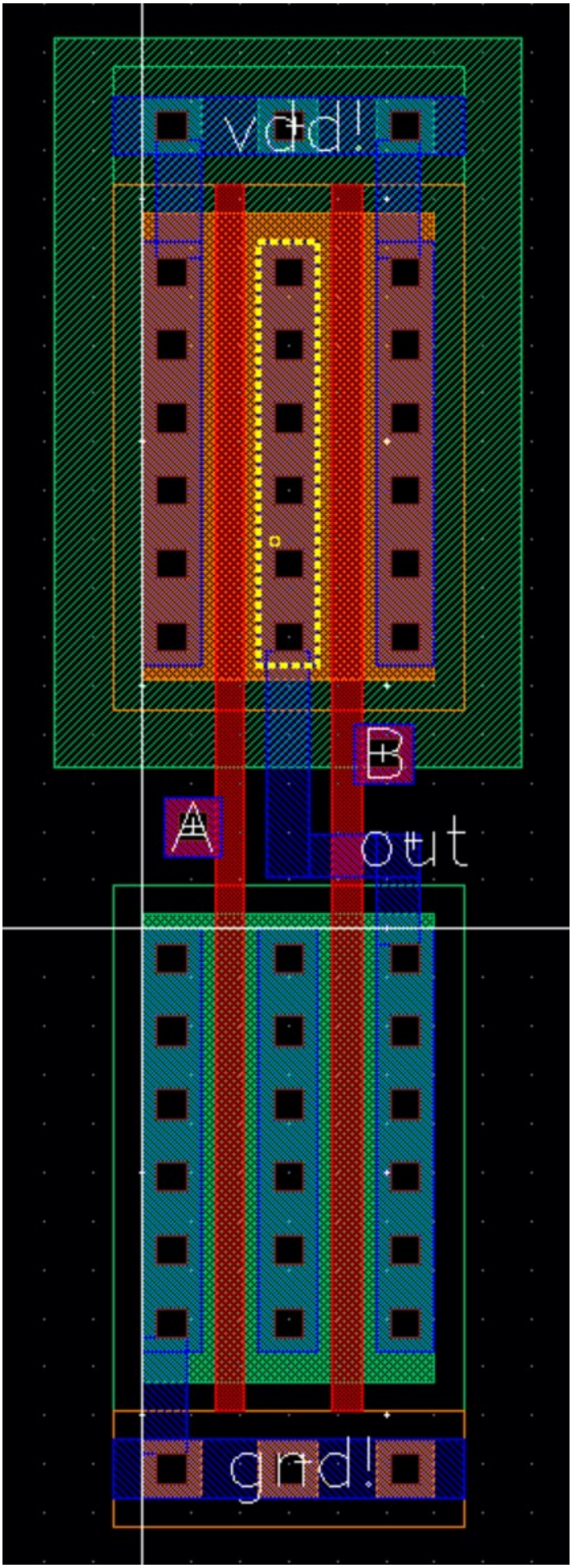

Fig. 47. Stage Y: NAND2, Layout

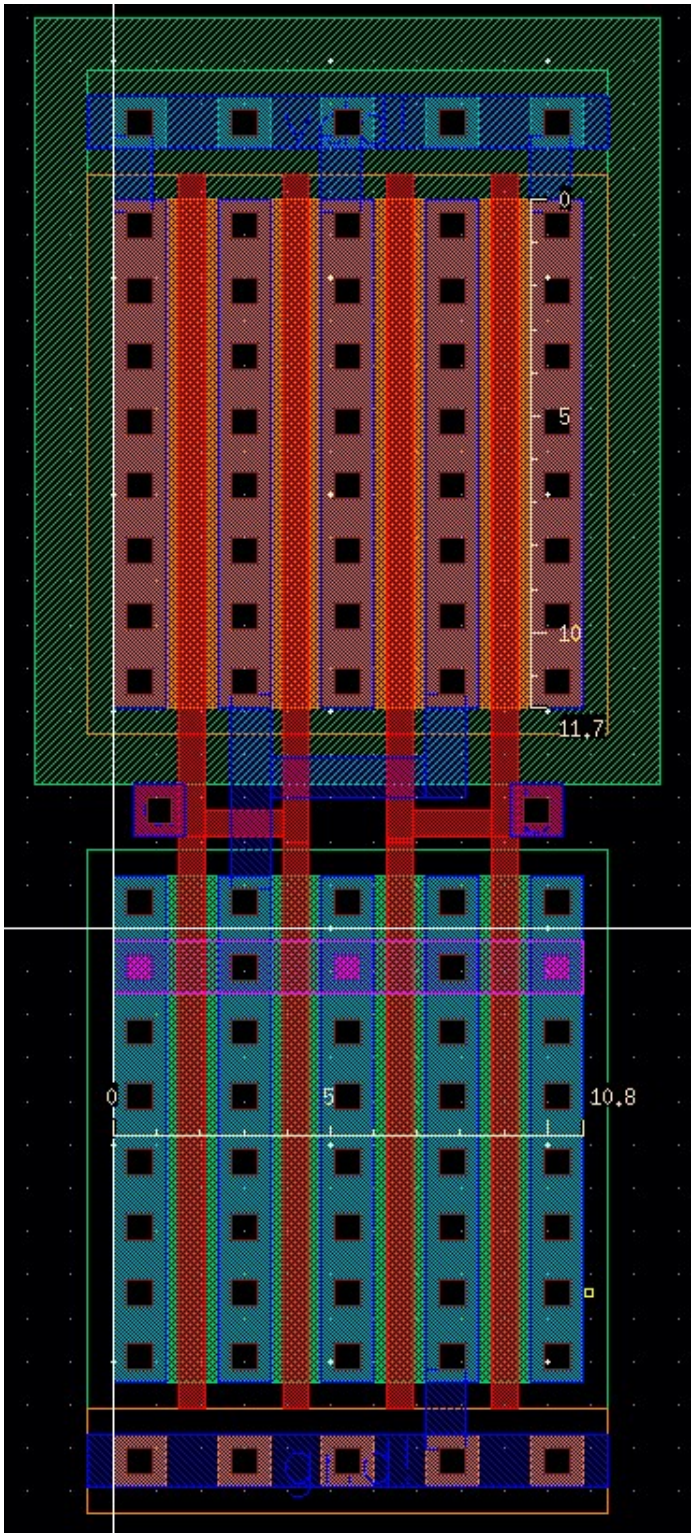

Fig. 48. Stage Z: NAND2, Layout

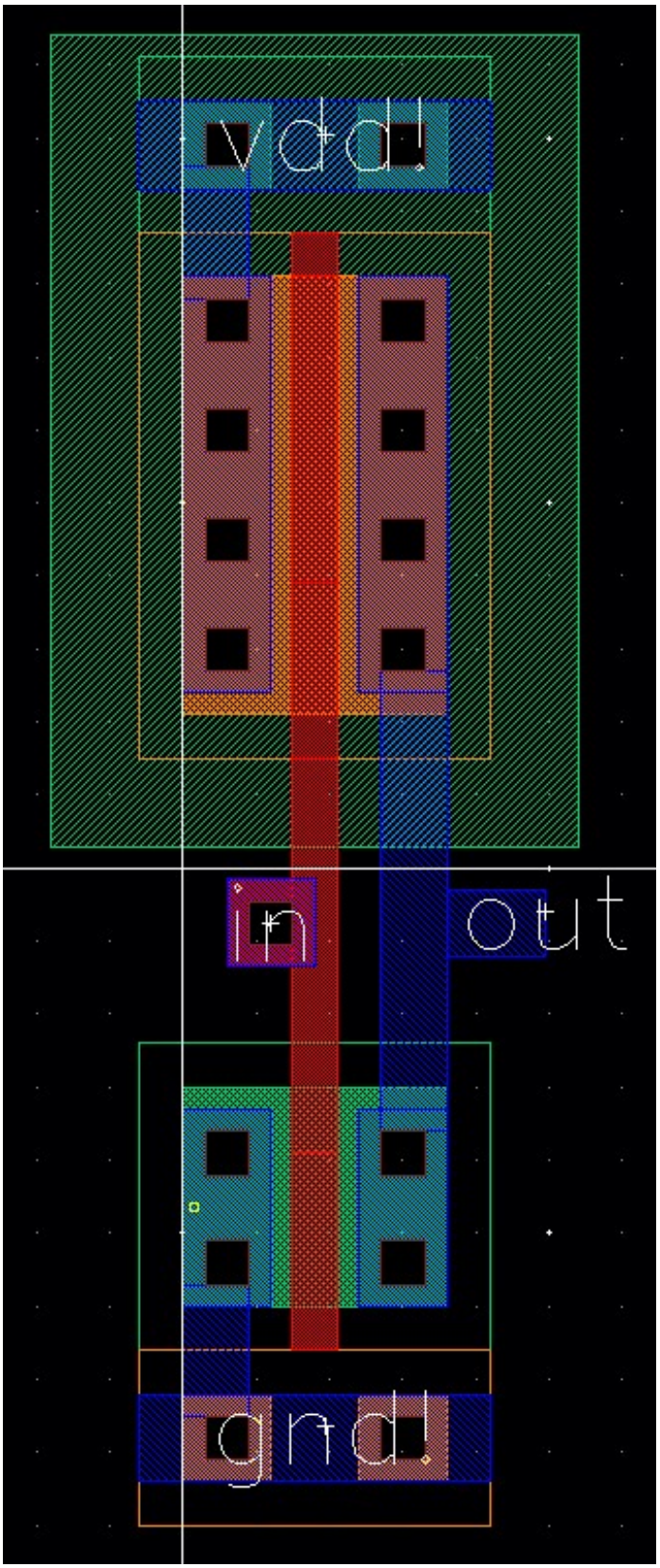

Fig. 49. Master Clock: Layout

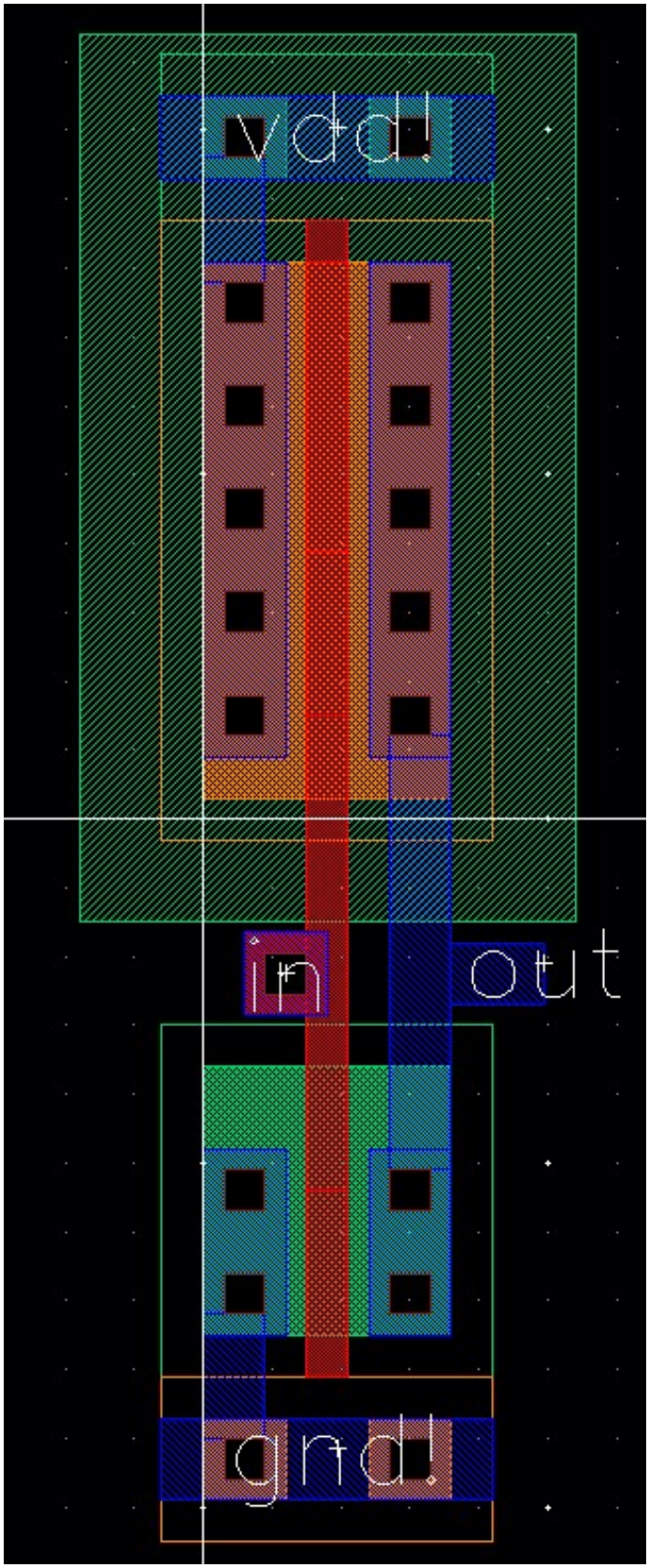

Fig. 50. Slave Clock: Layout

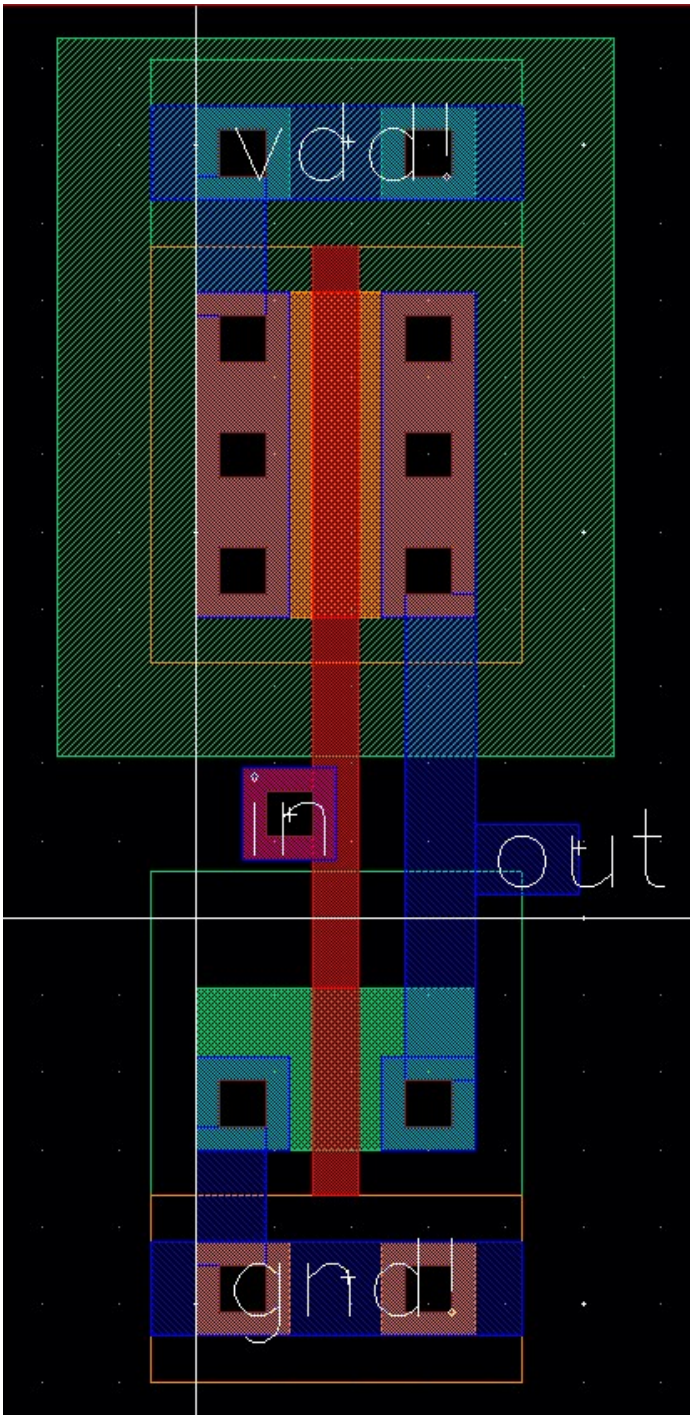

Fig. 51. Preset & Clear: Layout

APPENDIX F
INDIVIDUAL GATES EXTRACTED

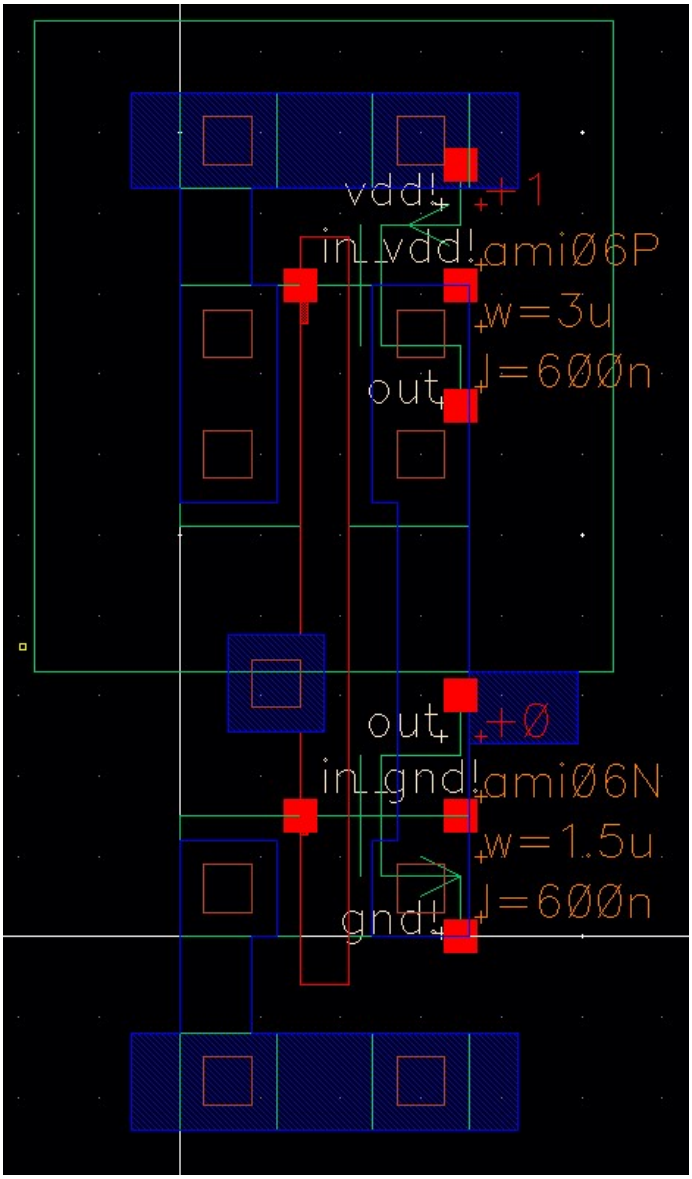

Fig. 52. Stage U: Inverter, Extracted

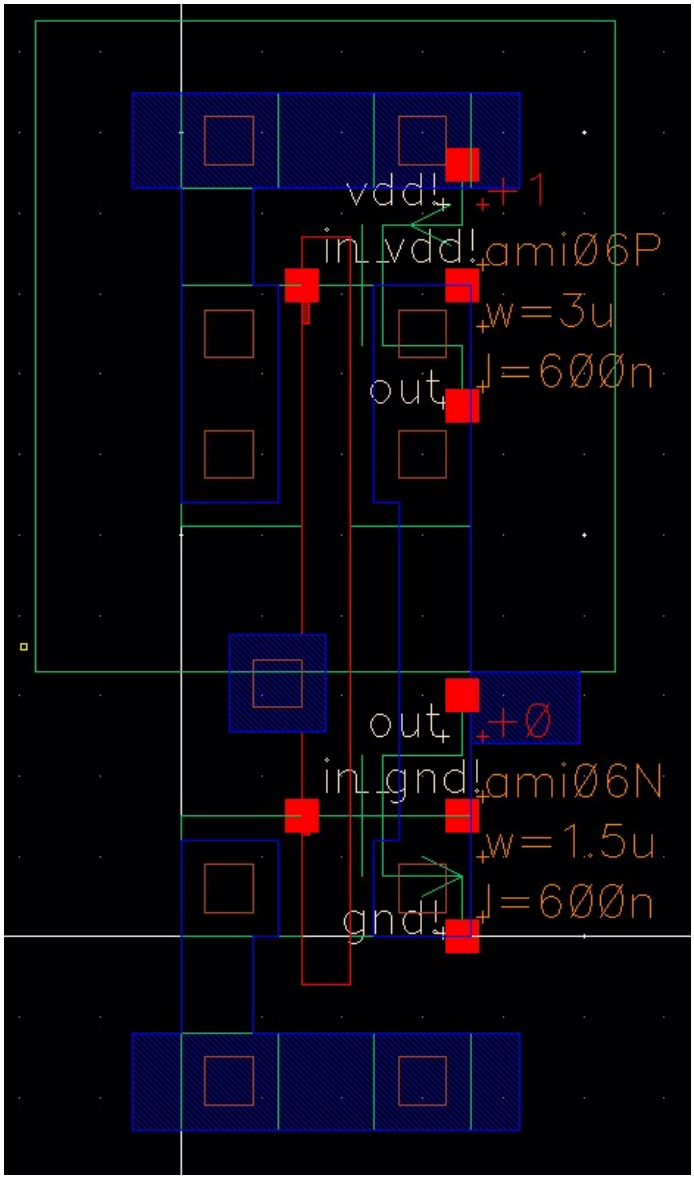

Fig. 53. Stage V: Inverter, Extracted

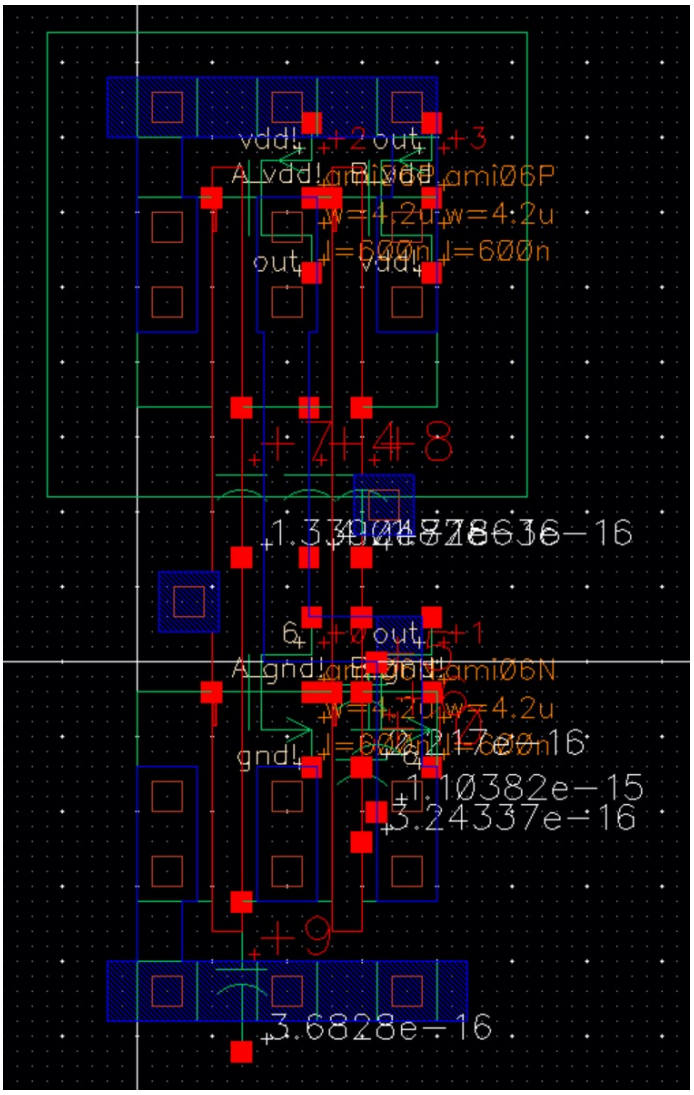

Fig. 54. Stage W: NAND2, Extracted

Fig. 55. Stage X: NAND3, Extracted

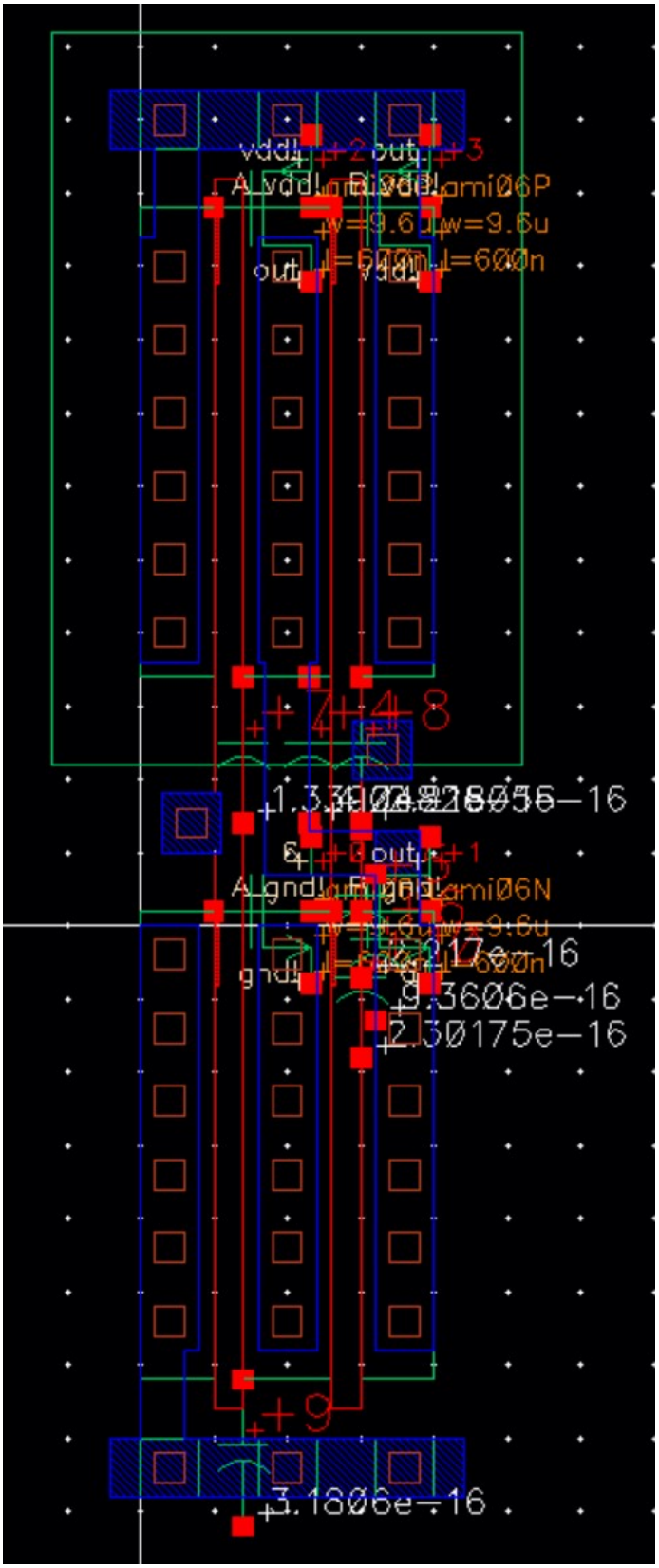

Fig. 56. Stage Y: NAND2, Extracted

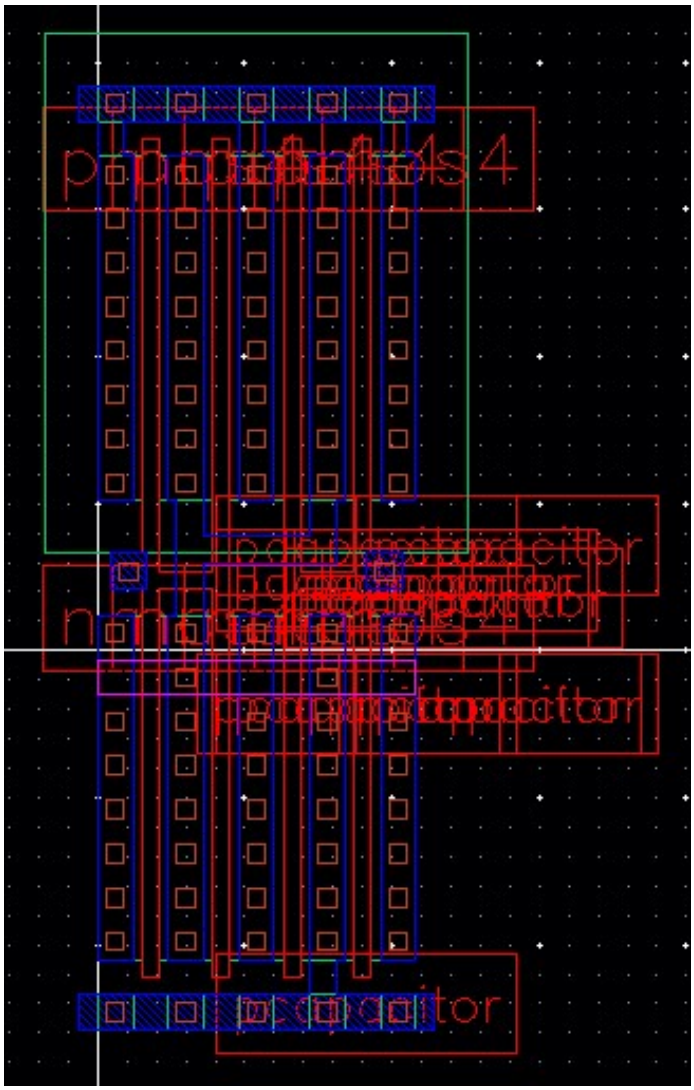

Fig. 57. Stage Z: NAND2, Extracted

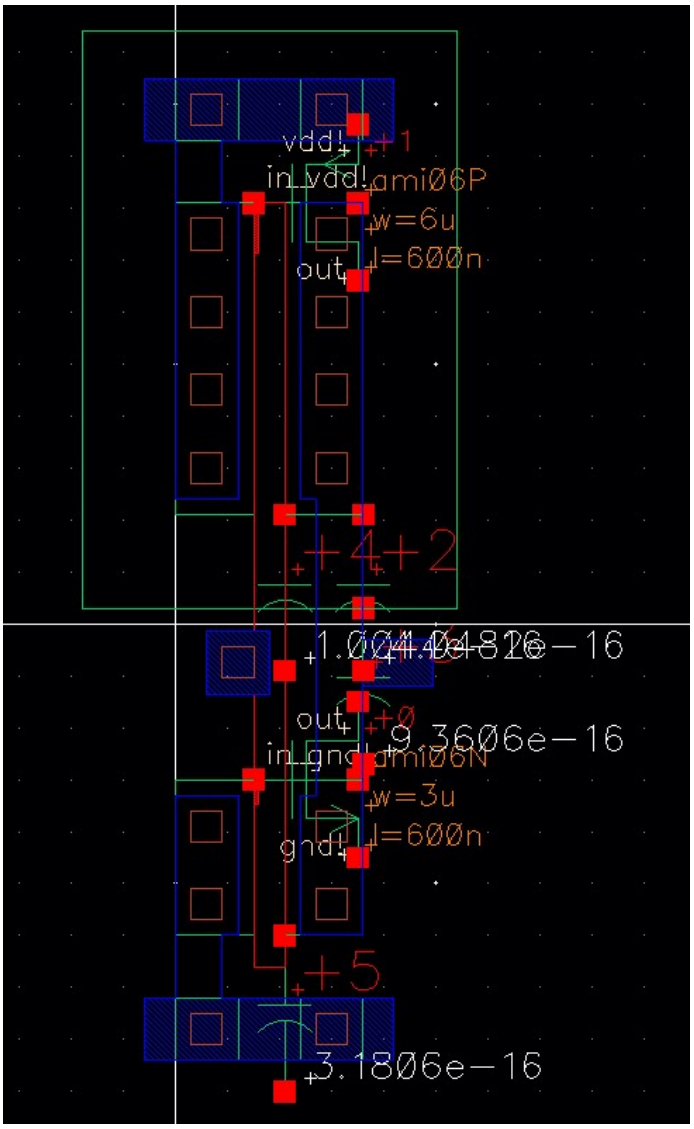

Fig. 58. Master Clock: Extracted

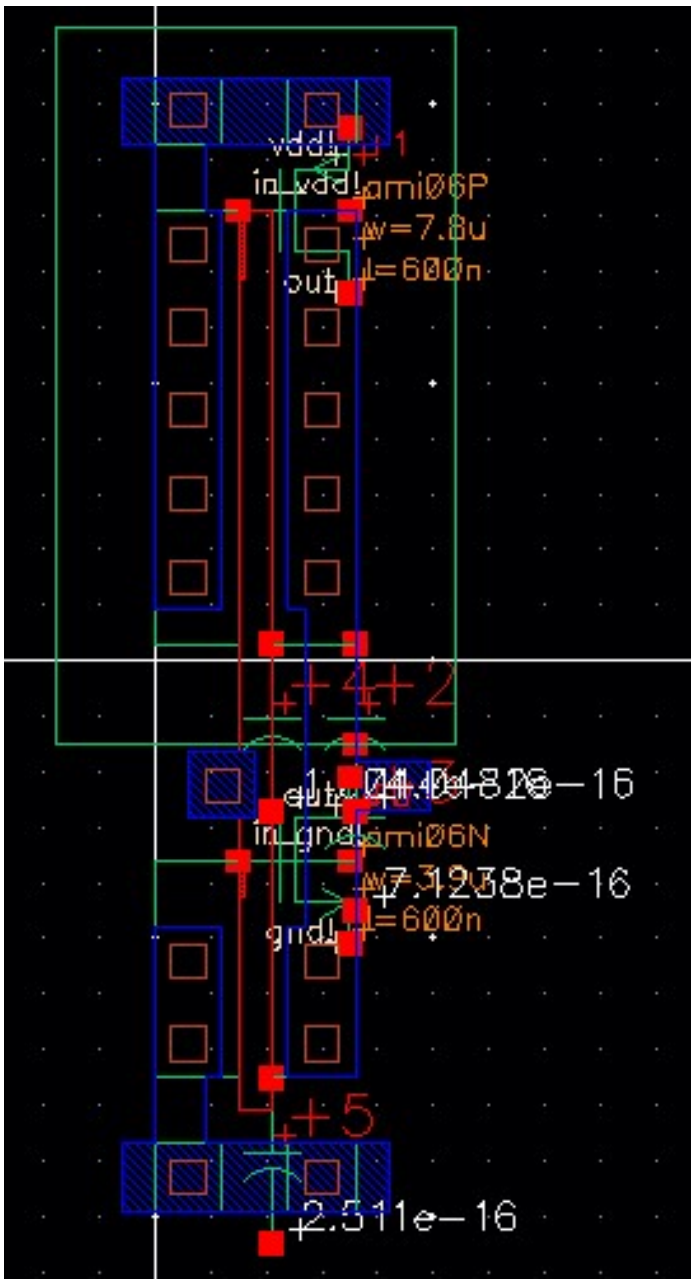

Fig. 59. Slave Clock: Extracted

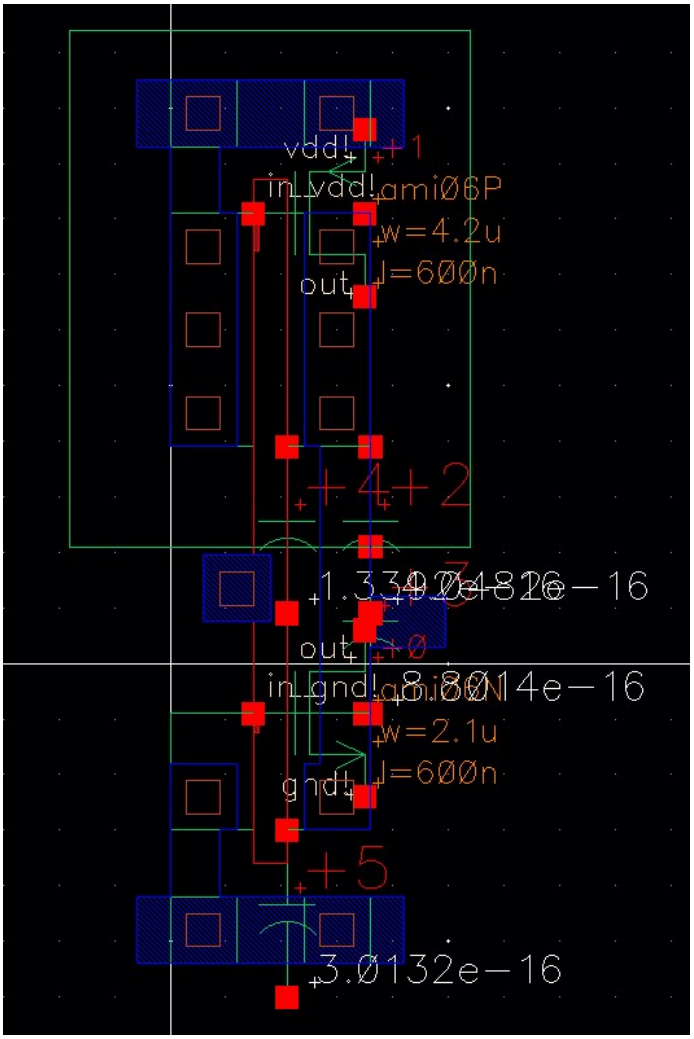

Fig. 60. Preset & Clear: Extracted

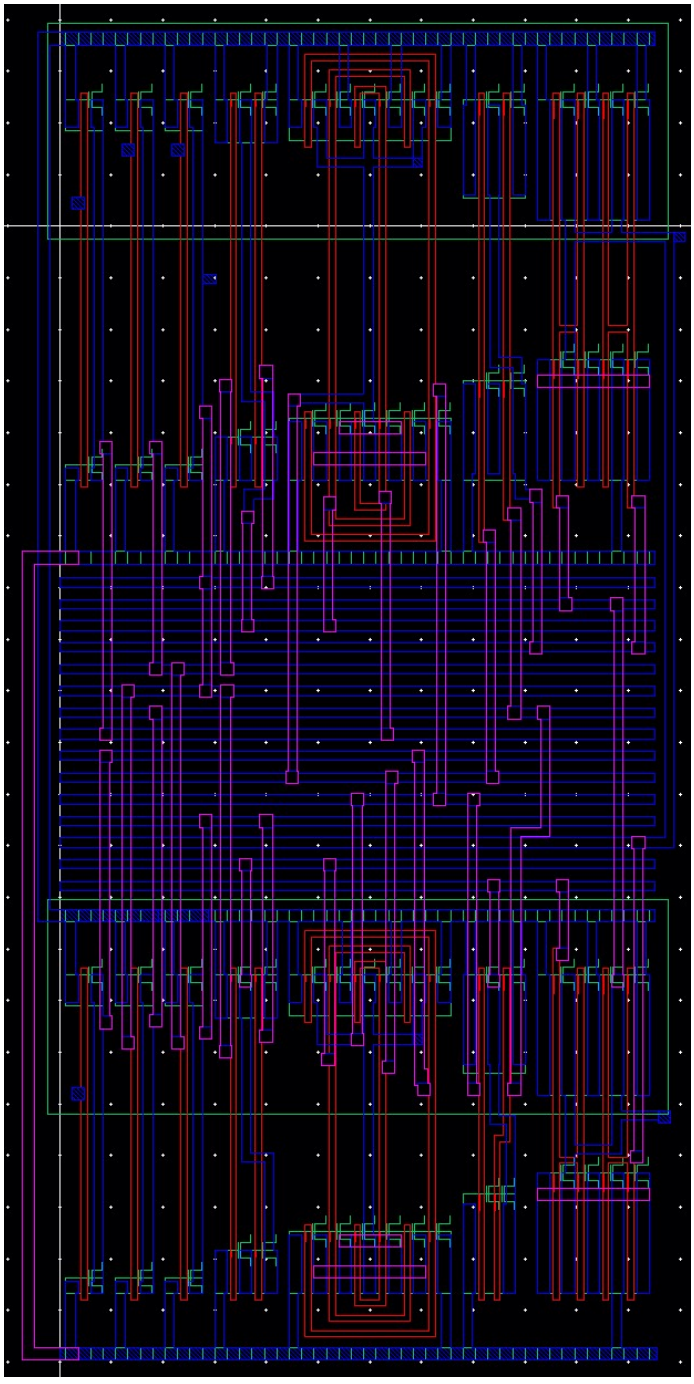

Fig. 61. Full Circuit Extracted

APPENDIX G
LAYOUT GATE SIMULATIONS

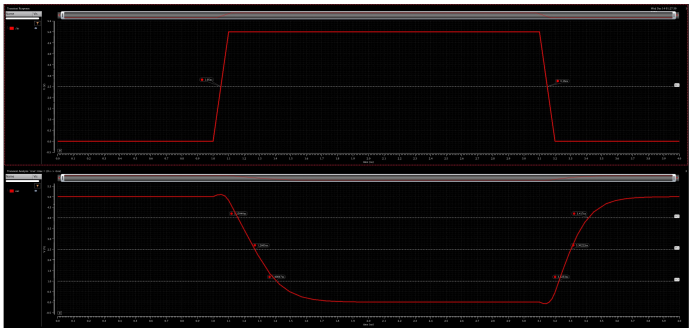

Fig. 62. Stage U: Inverter, Layout Simulation

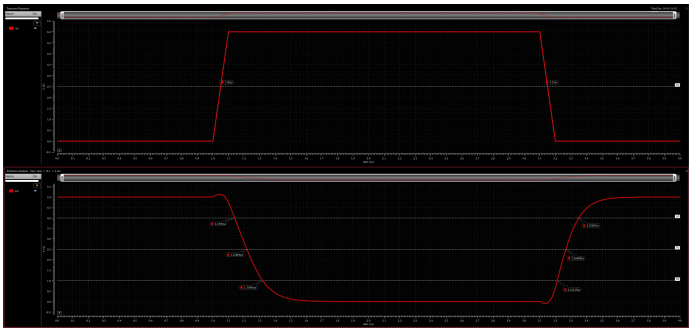

Fig. 63. Stage V: Inverter, Layout Simulation

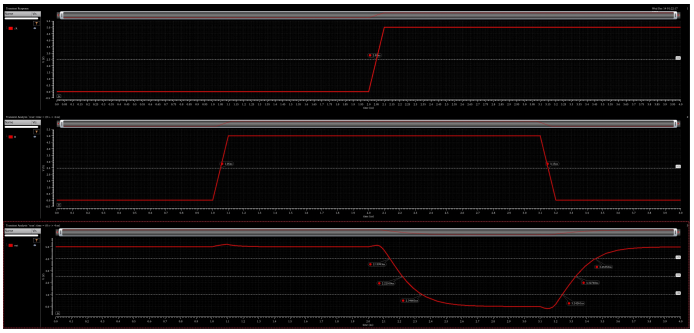

Fig. 64. Stage W: NAND2, Layout Simulation

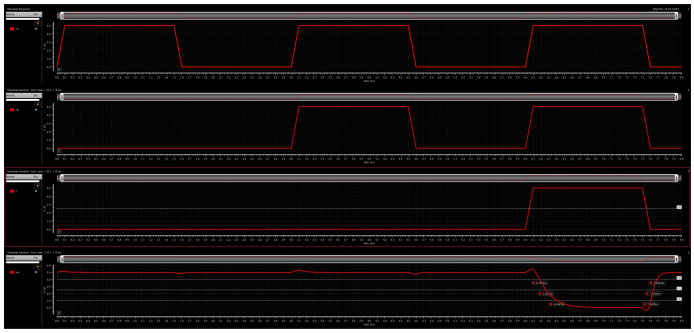

Fig. 65. Stage X: NAND3, Layout Simulation

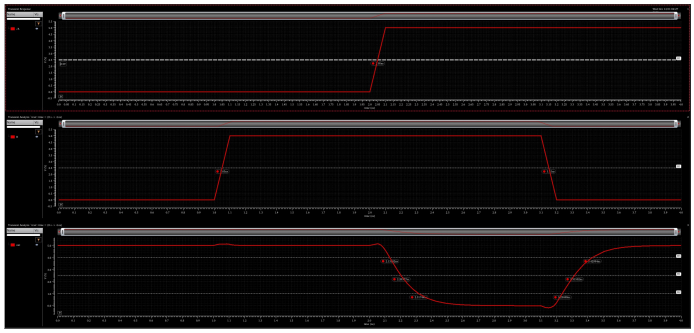

Fig. 66. Stage Y: NAND2, Layout Simulation

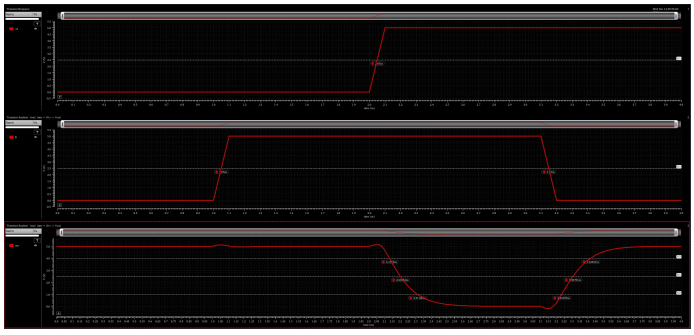

Fig. 67. Stage Z: NAND2, Layout Simulation

APPENDIX H
NETLISTS: SCHEMATIC SIMULATIONS

A. Stage U: Inverter, Schematic

```
// Point Netlist Generated on: Dec 14 00:38:00 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 00:38:00 2022
// Design library name: Project
// Design cell name: schemSim_UINV
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Library name: Project
// Cell name: V_INV
// View name: schematic
subckt V_INV in out
    N0 (out in 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u \
        pd=6u m=1 region=sat
    P0 (out in vdd! vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
        pd=9u m=1 region=sat
ends V_INV
// End of subcircuit definition.

// Library name: Project
// Cell name: schemSim_UINV
// View name: schematic
I0 (in out) V_INV
C0 (out 0) capacitor c=25.5927671f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=4n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save out in out in
saveOptions options save=allpub
```

B. Stage V: Inverter, Schematic

```
// Point Netlist Generated on: Dec 14 00:32:19 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 00:32:19 2022
// Design library name: Project
// Design cell name: schemSim_VINV
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Library name: Project
// Cell name: V_INV
// View name: schematic
subckt V_INV in out
    N0 (out in 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u \
        pd=6u m=1 region=sat
    P0 (out in vdd! vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
        pd=9u m=1 region=sat
ends V_INV
// End of subcircuit definition.

// Library name: Project
// Cell name: schemSim_VINV
// View name: schematic
I0 (in out) V_INV
C0 (out 0) capacitor c=16.5927671f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=4n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save out in out in
saveOptions options save=allpub
```

C. Stage W: NAND2, Schematic Simulation

```
// Point Netlist Generated on: Dec 14 00:24:14 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 00:23:57 2022
// Design library name: Project
// Design cell name: schemSim_W2NAND
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Library name: Project
// Cell name: W_2NAND
// View name: schematic
subckt W_2NAND A B out
    P1 (out B vdd! vdd!) ami06P w=4.2u l=600n as=6.3e-12 ad=6.3e-12 \
        ps=11.4u pd=11.4u m=1 region=sat
    P0 (out A vdd! vdd!) ami06P w=4.2u l=600n as=6.3e-12 ad=6.3e-12 \
        ps=11.4u pd=11.4u m=1 region=sat
    N1 (net1 B 0 0) ami06N w=4.2u l=600n as=6.3e-12 ad=6.3e-12 ps=11.4u \
        pd=11.4u m=1 region=sat
    N0 (out A net1 0) ami06N w=4.2u l=600n as=6.3e-12 ad=6.3e-12 ps=11.4u \
        pd=11.4u m=1 region=sat
ends W_2NAND
// End of subcircuit definition.

// Library name: Project
// Cell name: schemSim_W2NAND
// View name: schematic
I0 (A B out) W_2NAND
C0 (out 0) capacitor c=40.46422502f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=4n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save out A B out A B
saveOptions options save=allpub
```

D. Stage X: NAND3, Schematic Simulation

```
// Point Netlist Generated on: Dec 14 00:17:16 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 00:17:16 2022
// Design library name: Project
// Design cell name: schemSim_X3NAND
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Library name: Project
// Cell name: X_3NAND
// View name: schematic
subckt X_3NAND A B C out
    P5 (out C vdd! vdd!) ami06P w=4.05u l=600n as=6.075e-12 ad=6.075e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    P4 (out C vdd! vdd!) ami06P w=4.05u l=600n as=6.075e-12 ad=6.075e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    P3 (out B vdd! vdd!) ami06P w=4.05u l=600n as=6.075e-12 ad=6.075e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    P2 (out B vdd! vdd!) ami06P w=4.05u l=600n as=6.075e-12 ad=6.075e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    P1 (out A vdd! vdd!) ami06P w=4.05u l=600n as=6.075e-12 ad=6.075e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    P0 (out A vdd! vdd!) ami06P w=4.05u l=600n as=6.075e-12 ad=6.075e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    N5 (net2 C 0 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u pd=15.0u \
        m=1 region=sat
    N4 (net1 B net2 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    N3 (out A net1 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    N2 (net2 C 0 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u pd=15.0u \
        m=1 region=sat
    N1 (net1 B net2 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    N0 (out A net1 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
ends X_3NAND
// End of subcircuit definition.

// Library name: Project
// Cell name: schemSim_X3NAND
// View name: schematic
I0 (A B C out) X_3NAND
C0 (out 0) capacitor c=78.94299954f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=8n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save out A B C out C
saveOptions options save=allpub
```

E. Stage Y: NAND2, Schematic Simulation

```
// Point Netlist Generated on: Dec 14 00:10:22 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 00:10:22 2022
// Design library name: Project
// Design cell name: schemSim_Y2NAND
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Library name: Project
// Cell name: Y_2NAND
// View name: schematic
subckt Y_2NAND A B out
    P1 (out B vdd! vdd!) ami06P w=9.6u l=600n as=1.44e-11 ad=1.44e-11 \
        ps=22.2u pd=22.2u m=1 region=sat
    P0 (out A vdd! vdd!) ami06P w=9.6u l=600n as=1.44e-11 ad=1.44e-11 \
        ps=22.2u pd=22.2u m=1 region=sat
    N1 (net1 B 0 0) ami06N w=9.6u l=600n as=1.44e-11 ad=1.44e-11 ps=22.2u \
        pd=22.2u m=1 region=sat
    N0 (out A net1 0) ami06N w=9.6u l=600n as=1.44e-11 ad=1.44e-11 \
        ps=22.2u pd=22.2u m=1 region=sat
ends Y_2NAND
// End of subcircuit definition.

// Library name: Project
// Cell name: schemSim_Y2NAND
// View name: schematic
I0 (A B out) Y_2NAND
C0 (out 0) capacitor c=93.83689782f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=4n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save out A B out A B
saveOptions options save=allpub
```

F. Stage Z: NAND2, Schematic Simulation

```
// Point Netlist Generated on: Dec 14 00:03:13 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 00:01:50 2022
// Design library name: Project
// Design cell name: schemSim_Z2NAND
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Library name: Project
// Cell name: Z_2NAND
// View name: schematic
subckt Z_2NAND A B out
    P3 (out B vdd! vdd!) ami06P w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    P2 (out B vdd! vdd!) ami06P w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    P1 (out A vdd! vdd!) ami06P w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    P0 (out A vdd! vdd!) ami06P w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    N3 (net1 B 0 0) ami06N w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    N2 (out A net1 0) ami06N w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    N1 (net1 B 0 0) ami06N w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    N0 (out A net1 0) ami06N w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
ends Z_2NAND
// End of subcircuit definition.

// Library name: Project
// Cell name: schemSim_Z2NAND
// View name: schematic
I0 (A B out) Z_2NAND
C0 (out 0) capacitor c=228.8368978f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=4n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save out A B out B A
saveOptions options save=allpub
```

G. Full Circuit, Schematic Simulation

```
// Point Netlist Generated on: Dec 14 00:44:53 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 00:44:53 2022
// Design library name: Project
// Design cell name: FlipFlopTest
// Design view name: schematic
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Library name: Project
// Cell name: V_INV
// View name: schematic
subckt V_INV in out
    N0 (out in 0 0) ami06N w=1.5u l=600n as=2.25e-12 ad=2.25e-12 ps=6u \
        pd=6u m=1 region=sat
    P0 (out in vdd! vdd!) ami06P w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u \
        pd=9u m=1 region=sat
ends V_INV
// End of subcircuit definition.

// Library name: Project
// Cell name: W_2NAND
// View name: schematic
subckt W_2NAND A B out
    P1 (out B vdd! vdd!) ami06P w=4.2u l=600n as=6.3e-12 ad=6.3e-12 \
        ps=11.4u pd=11.4u m=1 region=sat
    P0 (out A vdd! vdd!) ami06P w=4.2u l=600n as=6.3e-12 ad=6.3e-12 \
        ps=11.4u pd=11.4u m=1 region=sat
    N1 (net1 B 0 0) ami06N w=4.2u l=600n as=6.3e-12 ad=6.3e-12 ps=11.4u \
        pd=11.4u m=1 region=sat
    N0 (out A net1 0) ami06N w=4.2u l=600n as=6.3e-12 ad=6.3e-12 ps=11.4u \
        pd=11.4u m=1 region=sat
ends W_2NAND
// End of subcircuit definition.

// Library name: Project
// Cell name: X_3NAND
// View name: schematic
subckt X_3NAND A B C out
    P5 (out C vdd! vdd!) ami06P w=4.05u l=600n as=6.075e-12 ad=6.075e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    P4 (out C vdd! vdd!) ami06P w=4.05u l=600n as=6.075e-12 ad=6.075e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    P3 (out B vdd! vdd!) ami06P w=4.05u l=600n as=6.075e-12 ad=6.075e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    P2 (out B vdd! vdd!) ami06P w=4.05u l=600n as=6.075e-12 ad=6.075e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    P1 (out A vdd! vdd!) ami06P w=4.05u l=600n as=6.075e-12 ad=6.075e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    P0 (out A vdd! vdd!) ami06P w=4.05u l=600n as=6.075e-12 ad=6.075e-12 \
        ps=11.1u pd=11.1u m=1 region=sat
    N5 (net2 C 0 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u pd=15.0u \
        m=1 region=sat
    N4 (net1 B net2 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    N3 (out A net1 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    N2 (net2 C 0 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u pd=15.0u \
        m=1 region=sat
    N1 (net1 B net2 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
    N0 (out A net1 0) ami06N w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
ends X_3NAND
// End of subcircuit definition.

// Library name: Project
// Cell name: Z_2NAND
```

```
// View name: schematic
subckt Z_2NAND A B out
    P3 (out B vdd! vdd!) ami06P w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    P2 (out B vdd! vdd!) ami06P w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    P1 (out A vdd! vdd!) ami06P w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    P0 (out A vdd! vdd!) ami06P w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    N3 (net1 B 0 0) ami06N w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    N2 (out A net1 0) ami06N w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    N1 (net1 B 0 0) ami06N w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
    N0 (out A net1 0) ami06N w=11.7u l=600n as=1.755e-11 ad=1.755e-11 \
        ps=26.4u pd=26.4u m=1 region=sat
ends Z_2NAND
// End of subcircuit definition.

// Library name: Project
// Cell name: Y_2NAND
// View name: schematic
subckt Y_2NAND A B out
    P1 (out B vdd! vdd!) ami06P w=9.6u l=600n as=1.44e-11 ad=1.44e-11 \
        ps=22.2u pd=22.2u m=1 region=sat
    P0 (out A vdd! vdd!) ami06P w=9.6u l=600n as=1.44e-11 ad=1.44e-11 \
        ps=22.2u pd=22.2u m=1 region=sat
    N1 (net1 B 0 0) ami06N w=9.6u l=600n as=1.44e-11 ad=1.44e-11 ps=22.2u \
        pd=22.2u m=1 region=sat
    N0 (out A net1 0) ami06N w=9.6u l=600n as=1.44e-11 ad=1.44e-11 \
        ps=22.2u pd=22.2u m=1 region=sat
ends Y_2NAND
// End of subcircuit definition.

// Library name: Project
// Cell name: PresetClear
// View name: schematic
subckt PresetClear in out
    N0 (out in 0 0) ami06N w=2.1u l=600n as=3.15e-12 ad=3.15e-12 ps=7.2u \
        pd=7.2u m=1 region=sat
    P0 (out in vdd! vdd!) ami06P w=4.2u l=600n as=6.3e-12 ad=6.3e-12 \
        ps=11.4u pd=11.4u m=1 region=sat
ends PresetClear
// End of subcircuit definition.

// Library name: Project
// Cell name: ClockMaster
// View name: schematic
subckt ClockMaster in out
    N0 (out in 0 0) ami06N w=3u l=600n as=4.5e-12 ad=4.5e-12 ps=9u pd=9u \
        m=1 region=sat
    P0 (out in vdd! vdd!) ami06P w=6u l=600n as=9e-12 ad=9e-12 ps=15.0u \
        pd=15.0u m=1 region=sat
ends ClockMaster
// End of subcircuit definition.

// Library name: Project
// Cell name: ClockSlave
// View name: schematic
subckt ClockSlave in out
    N0 (out in 0 0) ami06N w=3.9u l=600n as=5.85e-12 ad=5.85e-12 ps=10.8u \
        pd=10.8u m=1 region=sat
    P0 (out in vdd! vdd!) ami06P w=7.8u l=600n as=1.17e-11 ad=1.17e-11 \
        ps=18.6u pd=18.6u m=1 region=sat
ends ClockSlave
// End of subcircuit definition.

// Library name: Project
// Cell name: Design
// View name: schematic
subckt Design CLEAR CLK D PRESET Q Q_NOT CLK_NOT MASTER_Q MASTER_QNOT
    I25 (net1 net4) V_INV
```

```
    I34 (D net1) V_INV
    I22 (CLK_NOT net4 net5) W_2NAND
    I21 (net1 CLK_NOT net3) W_2NAND
    I20 (MASTER_QNOT net5 net6 MASTER_Q) X_3NAND
    I19 (net2 net3 MASTER_Q MASTER_QNOT) X_3NAND
    I31 (Q_NOT net11 Q) Z_2NAND
    I30 (net10 Q Q_NOT) Z_2NAND
    I18 (MASTER_Q net7 net11) Y_2NAND
    I17 (MASTER_QNOT net7 net10) Y_2NAND
    I44 (CLEAR net6) PresetClear
    I43 (PRESET net2) PresetClear
    I45 (CLK CLK_NOT) ClockMaster
    I46 (CLK_NOT net7) ClockSlave
ends Design
// End of subcircuit definition.

// Library name: Project
// Cell name: FlipFlopTest
// View name: schematic
I0 (CLEAR CLK D PRESET Q Q_NOT CLK_NOT MASTER_Q MASTER_QNOT) Design
C1 (Q 0) capacitor c=228.8368978f m=1
C0 (Q_NOT 0) capacitor c=228.8368978f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=24n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save Q Q_NOT CLK D Q CLK MASTER_Q D CLK_NOT C0:1 C0:1
saveOptions options save=allpub
```

APPENDIX I
NETLISTS: LAYOUT SIMULATIONS

A. Stage U: Inverter, Layout Simulation

```
// Point Netlist Generated on: Dec 14 01:26:53 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 01:26:53 2022
// Design library name: Project
// Design cell name: sim_UINV
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
// Library name: Project
// Cell name: V_INV
// View name: extracted
// View type: maskLayout
subckt V_INV in out
    \+1 (out in vdd! vdd!) ami06P w=3e-06 l=6e-07 as=4.5e-12 ad=4.5e-12 \
        ps=6e-06 pd=6e-06 m=1 region=sat
    \+5 (in 0) capacitor c=1.96695e-16 m=1
    \+4 (in vdd!) capacitor c=1.71585e-16 m=1
    \+3 (out 0) capacitor c=6.5646e-16 m=1
    \+2 (out vdd!) capacitor c=4.0482e-16 m=1
    \+0 (out in 0 0) ami06N w=1.5e-06 l=6e-07 as=2.25e-12 ad=2.25e-12 \
        ps=4.5e-06 pd=4.5e-06 m=1 region=sat
ends V_INV
// End of subcircuit definition.

// Library name: Project
// Cell name: sim_UINV
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
I0 (in out) V_INV
C0 (out 0) capacitor c=25.5927671f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=4n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save out in out in
saveOptions options save=allpub
```

B. Stage V: Inverter, Layout Simulation

```
// Point Netlist Generated on: Dec 14 01:16:21 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 01:16:20 2022
// Design library name: Project
// Design cell name: sim_VINV
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
// Library name: Project
// Cell name: V_INV
// View name: extracted
// View type: maskLayout
subckt V_INV in out
    \+1 (out in vdd! vdd!) ami06P w=3e-06 l=6e-07 as=4.5e-12 ad=4.5e-12 \
        ps=6e-06 pd=6e-06 m=1 region=sat
    \+5 (in 0) capacitor c=1.96695e-16 m=1
    \+4 (in vdd!) capacitor c=1.71585e-16 m=1
    \+3 (out 0) capacitor c=6.5646e-16 m=1
    \+2 (out vdd!) capacitor c=4.0482e-16 m=1
    \+0 (out in 0 0) ami06N w=1.5e-06 l=6e-07 as=2.25e-12 ad=2.25e-12 \
        ps=4.5e-06 pd=4.5e-06 m=1 region=sat
ends V_INV
// End of subcircuit definition.

// Library name: Project
// Cell name: sim_VINV
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
I0 (in out) V_INV
C0 (out 0) capacitor c=16.5927671f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=4n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save out in out in
saveOptions options save=allpub
```

C. Stage W: NAND2, Layout Simulation

```
// Point Netlist Generated on: Dec 14 01:21:56 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 01:21:56 2022
// Design library name: Project
// Design cell name: sim_W2NAND
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
// Library name: Project
// Cell name: W_2NAND
// View name: extracted
// View type: maskLayout
subckt W_2NAND A B out
    \+3 (vdd! B out vdd!) ami06P w=4.2e-06 l=6e-07 as=3.78e-12 ad=6.3e-12 \
        ps=1.8e-06 pd=7.2e-06 m=1 region=sat
    \+2 (out A vdd! vdd!) ami06P w=4.2e-06 l=6e-07 as=6.3e-12 ad=3.78e-12 \
        ps=7.2e-06 pd=1.8e-06 m=1 region=sat
    \+10 (B 0) capacitor c=3.24337e-16 m=1
    \+9 (A 0) capacitor c=3.6828e-16 m=1
    \+8 (vdd! B) capacitor c=1.77863e-16 m=1
    \+7 (vdd! A) capacitor c=1.3392e-16 m=1
    \+6 (out 0) capacitor c=1.10382e-15 m=1
    \+5 (out B) capacitor c=2.217e-16 m=1
    \+4 (out vdd!) capacitor c=4.0482e-16 m=1
    \+1 (out B 6 0) ami06N w=4.2e-06 l=6e-07 as=3.78e-12 ad=6.3e-12 \
        ps=1.8e-06 pd=7.2e-06 m=1 region=sat
    \+0 (6 A 0 0) ami06N w=4.2e-06 l=6e-07 as=6.3e-12 ad=3.78e-12 \
        ps=7.2e-06 pd=1.8e-06 m=1 region=sat
ends W_2NAND
// End of subcircuit definition.

// Library name: Project
// Cell name: sim_W2NAND
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
I0 (A B out) W_2NAND
C0 (out 0) capacitor c=40.46422502f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=4n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save out A B out A B
saveOptions options save=allpub
```

D. Stage X: NAND3, Layout Simulation

```
// Point Netlist Generated on: Dec 14 01:06:40 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 01:06:40 2022
// Design library name: Project
// Design cell name: sim_X3NAND
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
// Library name: Project
// Cell name: X_3NAND
// View name: extracted
// View type: maskLayout
subckt X_3NAND A B C out
    \+11 (vdd! C out vdd!) ami06P w=4.05e-06 l=6e-07 as=3.645e-12 \
        ad=6.075e-12 ps=1.8e-06 pd=7.05e-06 m=1 region=sat
    \+10 (out B vdd! vdd!) ami06P w=4.05e-06 l=6e-07 as=3.645e-12 \
        ad=3.645e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+9 (vdd! A out vdd!) ami06P w=4.05e-06 l=6e-07 as=3.645e-12 \
        ad=3.645e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+8 (out A vdd! vdd!) ami06P w=4.05e-06 l=6e-07 as=3.645e-12 \
        ad=3.645e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+7 (vdd! B out vdd!) ami06P w=4.05e-06 l=6e-07 as=3.645e-12 \
        ad=3.645e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+6 (out C vdd! vdd!) ami06P w=4.05e-06 l=6e-07 as=6.075e-12 \
        ad=3.645e-12 ps=7.05e-06 pd=1.8e-06 m=1 region=sat
    \+30 (C 0) capacitor c=1.53171e-15 m=1
    \+29 (B 0) capacitor c=1.09647e-15 m=1
    \+28 (A 0) capacitor c=6.6123e-16 m=1
    \+27 (vdd! C) capacitor c=1.23876e-15 m=1
    \+26 (vdd! B) capacitor c=8.0352e-16 m=1
    \+25 (vdd! A) capacitor c=3.6828e-16 m=1
    \+24 (vdd! C) capacitor c=4.434e-16 m=1
    \+23 (vdd! B) capacitor c=4.434e-16 m=1
    \+22 (out 0) capacitor c=3.11694e-15 m=1
    \+21 (out C) capacitor c=2.217e-16 m=1
    \+20 (out B) capacitor c=2.217e-16 m=1
    \+19 (out A) capacitor c=2.217e-16 m=1
    \+18 (out vdd!) capacitor c=1.21446e-15 m=1
    \+17 (7 8) capacitor c=6.744e-16 m=1
    \+16 (B 7) capacitor c=3.7008e-16 m=1
    \+15 (A 8) capacitor c=3.7008e-16 m=1
    \+14 (A 7) capacitor c=3.7008e-16 m=1
    \+13 (out 8) capacitor c=3.372e-16 m=1
    \+12 (out 7) capacitor c=3.372e-16 m=1
    \+5 (0 C 7 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 ad=9e-12 ps=1.8e-06 \
        pd=9e-06 m=1 region=sat
    \+4 (7 B 8 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 ad=5.4e-12 ps=1.8e-06 \
        pd=1.8e-06 m=1 region=sat
    \+3 (8 A out 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 ad=5.4e-12 \
        ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+2 (out A 8 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 ad=5.4e-12 \
        ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+1 (8 B 7 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 ad=5.4e-12 ps=1.8e-06 \
        pd=1.8e-06 m=1 region=sat
    \+0 (7 C 0 0) ami06N w=6e-06 l=6e-07 as=9e-12 ad=5.4e-12 ps=9e-06 \
        pd=1.8e-06 m=1 region=sat
ends X_3NAND
// End of subcircuit definition.

// Library name: Project
// Cell name: sim_X3NAND
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
I0 (A B C out) X_3NAND
```

```
C0 (out 0) capacitor c=78.94299954f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=8n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save out A B C out C
saveOptions options save=allpub
```

E. Stage Y: NAND2, Layout Simulation

```
// Point Netlist Generated on: Dec 14 01:01:19 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 01:01:19 2022
// Design library name: Project
// Design cell name: sim_Y2NAND
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
// Library name: Project
// Cell name: Y_2NAND
// View name: extracted
// View type: maskLayout
subckt Y_2NAND A B out
    \+3 (vdd! B out vdd!) ami06P w=9.6e-06 l=6e-07 as=8.64e-12 ad=1.44e-11 \
        ps=1.8e-06 pd=1.26e-05 m=1 region=sat
    \+2 (out A vdd! vdd!) ami06P w=9.6e-06 l=6e-07 as=1.44e-11 ad=8.64e-12 \
        ps=1.26e-05 pd=1.8e-06 m=1 region=sat
    \+10 (B 0) capacitor c=2.30175e-16 m=1
    \+9 (A 0) capacitor c=3.1806e-16 m=1
    \+8 (vdd! B) capacitor c=2.21805e-16 m=1
    \+7 (vdd! A) capacitor c=1.3392e-16 m=1
    \+6 (out 0) capacitor c=9.3606e-16 m=1
    \+5 (out B) capacitor c=2.217e-16 m=1
    \+4 (out vdd!) capacitor c=4.0482e-16 m=1
    \+1 (out B 6 0) ami06N w=9.6e-06 l=6e-07 as=8.64e-12 ad=1.44e-11 \
        ps=1.8e-06 pd=1.26e-05 m=1 region=sat
    \+0 (6 A 0 0) ami06N w=9.6e-06 l=6e-07 as=1.44e-11 ad=8.64e-12 \
        ps=1.26e-05 pd=1.8e-06 m=1 region=sat
ends Y_2NAND
// End of subcircuit definition.

// Library name: Project
// Cell name: sim_Y2NAND
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
I0 (A B out) Y_2NAND
C0 (out 0) capacitor c=93.83689782f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=4n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save out B A out A B C0:1 C0:1
saveOptions options save=allpub
```

F. Stage Z: NAND2, Layout Simulation

```
// Point Netlist Generated on: Dec 14 00:55:17 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 00:55:03 2022
// Design library name: Project
// Design cell name: sim_Z2NAND
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
// Library name: Project
// Cell name: Z_2NAND
// View name: extracted
// View type: maskLayout
subckt Z_2NAND A B out
    \+7 (vdd! A out vdd!) ami06P w=1.17e-05 l=6e-07 as=1.053e-11 \
        ad=1.755e-11 ps=1.8e-06 pd=1.47e-05 m=1 region=sat
    \+6 (out A vdd! vdd!) ami06P w=1.17e-05 l=6e-07 as=1.053e-11 \
        ad=1.053e-11 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+5 (vdd! B out vdd!) ami06P w=1.17e-05 l=6e-07 as=1.053e-11 \
        ad=1.053e-11 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+4 (out B vdd! vdd!) ami06P w=1.17e-05 l=6e-07 as=1.755e-11 \
        ad=1.053e-11 ps=1.47e-05 pd=1.8e-06 m=1 region=sat
    \+19 (B 0) capacitor c=5.022e-16 m=1
    \+18 (A 0) capacitor c=5.022e-16 m=1
    \+17 (vdd! B) capacitor c=2.6784e-16 m=1
    \+16 (vdd! A) capacitor c=2.6784e-16 m=1
    \+15 (out 0) capacitor c=8.9274e-16 m=1
    \+14 (out B) capacitor c=4.434e-16 m=1
    \+13 (out A) capacitor c=2.217e-16 m=1
    \+12 (out vdd!) capacitor c=1.13868e-15 m=1
    \+11 (0 6) capacitor c=3.372e-16 m=1
    \+10 (B 6) capacitor c=3.7008e-16 m=1
    \+9 (A 6) capacitor c=3.7008e-16 m=1
    \+8 (out 6) capacitor c=3.372e-16 m=1
    \+3 (6 A 0 0) ami06N w=1.17e-05 l=6e-07 as=1.053e-11 ad=1.755e-11 \
        ps=1.8e-06 pd=1.47e-05 m=1 region=sat
    \+2 (0 A 6 0) ami06N w=1.17e-05 l=6e-07 as=1.053e-11 ad=1.053e-11 \
        ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+1 (6 B out 0) ami06N w=1.17e-05 l=6e-07 as=1.053e-11 ad=1.053e-11 \
        ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+0 (out B 6 0) ami06N w=1.17e-05 l=6e-07 as=1.755e-11 ad=1.053e-11 \
        ps=1.47e-05 pd=1.8e-06 m=1 region=sat
ends Z_2NAND
// End of subcircuit definition.

// Library name: Project
// Cell name: sim_Z2NAND
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
I0 (A B out) Z_2NAND
C0 (out 0) capacitor c=228.8368978f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=4n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
```

```
save out A B out B A
saveOptions options save=allpub
```

G. Snap-Together Layout Simulation

```
// Point Netlist Generated on: Dec 14 01:36:03 2022
// Generated for: spectre
// Design Netlist Generated on: Dec 14 01:34:42 2022
// Design library name: Project
// Design cell name: sim_Design
// Design view name: config
simulator lang=spectre
global 0 vdd!
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06N.m"
include "/home/angelinic0/ncsu-cdk-1.6.0.beta/models/spectre/standalone/ami06P.m"

// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
// Library name: Project
// Cell name: Design
// View name: extracted
// View type: maskLayout
subckt Design CLEAR CLK D PRESET Q Q_NOT CLK_NOT MASTER_Q MASTER_QNOT
    \+67 (vdd! 27 Q_NOT vdd!) ami06P w=1.17e-05 l=6e-07 as=1.053e-11 \
        ad=1.755e-11 ps=1.8e-06 pd=1.47e-05 m=1 region=sat
    \+66 (vdd! Q_NOT Q vdd!) ami06P w=1.17e-05 l=6e-07 as=1.053e-11 \
        ad=1.755e-11 ps=1.8e-06 pd=1.47e-05 m=1 region=sat
    \+65 (Q_NOT 27 vdd! vdd!) ami06P w=1.17e-05 l=6e-07 as=1.053e-11 \
        ad=1.053e-11 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+64 (Q Q_NOT vdd! vdd!) ami06P w=1.17e-05 l=6e-07 as=1.053e-11 \
        ad=1.053e-11 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+63 (vdd! Q Q_NOT vdd!) ami06P w=1.17e-05 l=6e-07 as=1.053e-11 \
        ad=1.053e-11 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+62 (vdd! 26 Q vdd!) ami06P w=1.17e-05 l=6e-07 as=1.053e-11 \
        ad=1.053e-11 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+61 (Q_NOT Q vdd! vdd!) ami06P w=1.17e-05 l=6e-07 as=1.755e-11 \
        ad=1.053e-11 ps=1.47e-05 pd=1.8e-06 m=1 region=sat
    \+60 (Q 26 vdd! vdd!) ami06P w=1.17e-05 l=6e-07 as=1.755e-11 \
        ad=1.053e-11 ps=1.47e-05 pd=1.8e-06 m=1 region=sat
    \+265 (0 27) capacitor c=1.70748e-15 m=1
    \+264 (0 26) capacitor c=8.0352e-16 m=1
    \+263 (0 20) capacitor c=1.3392e-15 m=1
    \+262 (0 19) capacitor c=1.9251e-15 m=1
    \+261 (0 16) capacitor c=7.7004e-16 m=1
    \+260 (0 15) capacitor c=1.62378e-15 m=1
    \+259 (0 14) capacitor c=2.14272e-15 m=1
    \+258 (0 13) capacitor c=1.77444e-15 m=1
    \+257 (0 12) capacitor c=1.48986e-15 m=1
    \+256 (MASTER_QNOT 0) capacitor c=2.12598e-15 m=1
    \+255 (Q 0) capacitor c=1.69074e-15 m=1
    \+254 (CLK 0) capacitor c=1.1718e-15 m=1
    \+253 (D 0) capacitor c=1.2555e-15 m=1
    \+252 (vdd! 27) capacitor c=2.6784e-16 m=1
    \+251 (vdd! 26) capacitor c=4.7709e-16 m=1
    \+250 (vdd! 20) capacitor c=1.31409e-15 m=1
    \+249 (vdd! 19) capacitor c=1.24713e-15 m=1
    \+248 (vdd! 16) capacitor c=6.696e-16 m=1
    \+247 (vdd! 15) capacitor c=6.1938e-16 m=1
    \+246 (vdd! 14) capacitor c=1.27224e-15 m=1
    \+245 (vdd! 13) capacitor c=1.78281e-15 m=1
    \+244 (vdd! 12) capacitor c=7.9515e-16 m=1
    \+243 (vdd! MASTER_QNOT) capacitor c=1.14669e-15 m=1
    \+242 (vdd! Q) capacitor c=2.6784e-16 m=1
    \+241 (vdd! CLK) capacitor c=5.5242e-16 m=1
    \+240 (vdd! D) capacitor c=7.1982e-16 m=1
    \+239 (MASTER_Q 0) capacitor c=2.87928e-15 m=1
    \+238 (MASTER_Q vdd!) capacitor c=2.05065e-15 m=1
    \+237 (Q_NOT 0) capacitor c=9.0396e-16 m=1
    \+236 (Q_NOT vdd!) capacitor c=2.6784e-16 m=1
    \+235 (CLEAR 0) capacitor c=8.8722e-16 m=1
    \+234 (CLEAR vdd!) capacitor c=6.5286e-16 m=1
    \+233 (CLK_NOT 0) capacitor c=2.77884e-15 m=1
    \+232 (CLK_NOT vdd!) capacitor c=1.674e-15 m=1
    \+231 (PRESET 0) capacitor c=1.22202e-15 m=1
    \+230 (PRESET vdd!) capacitor c=6.5286e-16 m=1
```

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\+229 (16 20) capacitor c=2.217e-16 m=1
\+228 (15 27) capacitor c=2.217e-16 m=1
\+227 (15 26) capacitor c=4.60125e-16 m=1
\+226 (0 27) capacitor c=1.47143e-14 m=1
\+225 (0 26) capacitor c=1.25907e-14 m=1
\+224 (0 20) capacitor c=1.38309e-14 m=1
\+223 (0 19) capacitor c=1.62241e-14 m=1
\+222 (0 16) capacitor c=1.40266e-14 m=1
\+221 (0 15) capacitor c=1.36384e-14 m=1
\+220 (0 14) capacitor c=1.53817e-14 m=1
\+219 (0 13) capacitor c=1.39148e-14 m=1
\+218 (0 12) capacitor c=1.52107e-14 m=1
\+217 (MASTER_QNOT 19) capacitor c=4.434e-16 m=1
\+216 (MASTER_QNOT 12) capacitor c=2.217e-16 m=1
\+215 (MASTER_QNOT 0) capacitor c=1.56827e-14 m=1
\+214 (Q 26) capacitor c=4.434e-16 m=1
\+213 (Q 0) capacitor c=1.40339e-14 m=1
\+212 (vdd! 27) capacitor c=7.9626e-16 m=1
\+211 (vdd! 26) capacitor c=7.9626e-16 m=1
\+210 (vdd! 20) capacitor c=2.24622e-15 m=1
\+209 (vdd! 19) capacitor c=2.24622e-15 m=1
\+208 (vdd! 16) capacitor c=2.20398e-15 m=1
\+207 (vdd! 15) capacitor c=1.30926e-15 m=1
\+206 (vdd! 14) capacitor c=2.0265e-15 m=1
\+205 (vdd! 13) capacitor c=2.4237e-15 m=1
\+204 (vdd! 12) capacitor c=1.80282e-15 m=1
\+203 (vdd! 0) capacitor c=1.69256e-14 m=1
\+202 (vdd! MASTER_QNOT) capacitor c=3.81714e-15 m=1
\+201 (vdd! Q) capacitor c=1.45236e-15 m=1
\+200 (MASTER_Q 20) capacitor c=2.217e-16 m=1
\+199 (MASTER_Q 0) capacitor c=1.3247e-14 m=1
\+198 (MASTER_Q MASTER_QNOT) capacitor c=2.217e-16 m=1
\+197 (MASTER_Q vdd!) capacitor c=4.32942e-15 m=1
\+196 (Q_NOT 27) capacitor c=4.434e-16 m=1
\+195 (Q_NOT 0) capacitor c=2.56208e-14 m=1
\+194 (Q_NOT Q) capacitor c=8.868e-16 m=1
\+193 (Q_NOT vdd!) capacitor c=1.82352e-15 m=1
\+192 (CLK_NOT 19) capacitor c=2.217e-16 m=1
\+191 (CLK_NOT 0) capacitor c=2.63473e-14 m=1
\+190 (CLK_NOT vdd!) capacitor c=1.4673e-15 m=1
\+189 (27 28) capacitor c=3.7008e-16 m=1
\+188 (26 29) capacitor c=3.7008e-16 m=1
\+187 (22 24) capacitor c=6.744e-16 m=1
\+186 (21 23) capacitor c=6.744e-16 m=1
\+185 (20 26) capacitor c=4.5828e-16 m=1
\+184 (20 22) capacitor c=3.7008e-16 m=1
\+183 (19 27) capacitor c=4.5828e-16 m=1
\+182 (19 21) capacitor c=3.7008e-16 m=1
\+181 (16 26) capacitor c=4.5828e-16 m=1
\+180 (16 20) capacitor c=4.5828e-16 m=1
\+179 (15 27) capacitor c=2.2914e-16 m=1
\+178 (15 26) capacitor c=4.5828e-16 m=1
\+177 (15 20) capacitor c=4.5828e-16 m=1
\+176 (15 19) capacitor c=2.2914e-16 m=1
\+175 (15 16) capacitor c=4.5828e-16 m=1
\+174 (14 27) capacitor c=4.5828e-16 m=1
\+173 (14 26) capacitor c=2.2914e-16 m=1
\+172 (14 20) capacitor c=2.2914e-16 m=1
\+171 (14 19) capacitor c=4.5828e-16 m=1
\+170 (14 16) capacitor c=2.2914e-16 m=1
\+169 (14 15) capacitor c=4.5828e-16 m=1
\+168 (13 26) capacitor c=4.5828e-16 m=1
\+167 (13 20) capacitor c=6.1116e-16 m=1
\+166 (13 16) capacitor c=4.5828e-16 m=1
\+165 (13 15) capacitor c=4.5828e-16 m=1
\+164 (13 14) capacitor c=2.2914e-16 m=1
\+163 (12 27) capacitor c=4.5828e-16 m=1
\+162 (12 23) capacitor c=3.7008e-16 m=1
\+161 (12 21) capacitor c=3.7008e-16 m=1
\+160 (12 19) capacitor c=6.1116e-16 m=1
\+159 (12 15) capacitor c=9.1656e-16 m=1
\+158 (12 14) capacitor c=6.8742e-16 m=1
\+157 (0 29) capacitor c=3.372e-16 m=1
\+156 (0 28) capacitor c=3.372e-16 m=1
```

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\+155 (0 27) capacitor c=2.75538e-15 m=1
\+154 (0 26) capacitor c=2.6835e-16 m=1
\+153 (0 20) capacitor c=5.5371e-16 m=1
\+152 (0 19) capacitor c=2.0467e-15 m=1
\+151 (0 16) capacitor c=1.12443e-15 m=1
\+150 (0 15) capacitor c=4.51748e-15 m=1
\+149 (0 14) capacitor c=7.24961e-15 m=1
\+148 (0 13) capacitor c=1.98051e-15 m=1
\+147 (0 12) capacitor c=4.36053e-15 m=1
\+146 (MASTER_QNOT 27) capacitor c=4.5828e-16 m=1
\+145 (MASTER_QNOT 26) capacitor c=2.2914e-16 m=1
\+144 (MASTER_QNOT 24) capacitor c=3.7008e-16 m=1
\+143 (MASTER_QNOT 23) capacitor c=3.372e-16 m=1
\+142 (MASTER_QNOT 22) capacitor c=3.7008e-16 m=1
\+141 (MASTER_QNOT 21) capacitor c=3.372e-16 m=1
\+140 (MASTER_QNOT 20) capacitor c=3.2166e-16 m=1
\+139 (MASTER_QNOT 19) capacitor c=4.5828e-16 m=1
\+138 (MASTER_QNOT 16) capacitor c=2.2914e-16 m=1
\+137 (MASTER_QNOT 15) capacitor c=9.1656e-16 m=1
\+136 (MASTER_QNOT 14) capacitor c=6.8742e-16 m=1
\+135 (MASTER_QNOT 13) capacitor c=1.00908e-15 m=1
\+134 (MASTER_QNOT 12) capacitor c=4.5828e-16 m=1
\+133 (MASTER_QNOT 0) capacitor c=6.91892e-15 m=1
\+132 (Q 29) capacitor c=3.372e-16 m=1
\+131 (Q 28) capacitor c=3.7008e-16 m=1
\+130 (Q 27) capacitor c=6.8742e-16 m=1
\+129 (Q 26) capacitor c=2.2914e-16 m=1
\+128 (Q 20) capacitor c=2.2914e-16 m=1
\+127 (Q 19) capacitor c=6.8742e-16 m=1
\+126 (Q 16) capacitor c=2.2914e-16 m=1
\+125 (Q 15) capacitor c=4.5828e-16 m=1
\+124 (Q 14) capacitor c=6.8742e-16 m=1
\+123 (Q 13) capacitor c=2.2914e-16 m=1
\+122 (Q 12) capacitor c=6.8742e-16 m=1
\+121 (Q 0) capacitor c=3.04567e-15 m=1
\+120 (Q MASTER_QNOT) capacitor c=6.8742e-16 m=1
\+119 (vdd! 26) capacitor c=1.75744e-15 m=1
\+118 (vdd! 20) capacitor c=1.89363e-15 m=1
\+117 (vdd! 16) capacitor c=3.78385e-15 m=1
\+116 (vdd! 15) capacitor c=4.8392e-15 m=1
\+115 (vdd! 14) capacitor c=2.14335e-15 m=1
\+114 (vdd! 13) capacitor c=3.23504e-15 m=1
\+113 (vdd! 0) capacitor c=3.1776e-16 m=1
\+112 (vdd! MASTER_QNOT) capacitor c=2.14725e-15 m=1
\+111 (vdd! Q) capacitor c=1.03032e-15 m=1
\+110 (MASTER_Q 27) capacitor c=2.2914e-16 m=1
\+109 (MASTER_Q 26) capacitor c=4.5828e-16 m=1
\+108 (MASTER_Q 24) capacitor c=3.372e-16 m=1
\+107 (MASTER_Q 22) capacitor c=3.372e-16 m=1
\+106 (MASTER_Q 20) capacitor c=1.55814e-15 m=1
\+105 (MASTER_Q 19) capacitor c=3.8202e-16 m=1
\+104 (MASTER_Q 16) capacitor c=4.5828e-16 m=1
\+103 (MASTER_Q 15) capacitor c=6.8742e-16 m=1
\+102 (MASTER_Q 14) capacitor c=4.5828e-16 m=1
\+101 (MASTER_Q 13) capacitor c=1.88846e-15 m=1
\+100 (MASTER_Q 12) capacitor c=3.8202e-16 m=1
\+99 (MASTER_Q 0) capacitor c=5.63718e-15 m=1
\+98 (MASTER_Q MASTER_QNOT) capacitor c=1.38702e-15 m=1
\+97 (MASTER_Q Q) capacitor c=4.5828e-16 m=1
\+96 (MASTER_Q vdd!) capacitor c=3.80227e-15 m=1
\+95 (Q_NOT 29) capacitor c=3.7008e-16 m=1
\+94 (Q_NOT 28) capacitor c=3.372e-16 m=1
\+93 (Q_NOT 26) capacitor c=2.2914e-16 m=1
\+92 (Q_NOT 20) capacitor c=2.2914e-16 m=1
\+91 (Q_NOT 16) capacitor c=4.5828e-16 m=1
\+90 (Q_NOT 15) capacitor c=4.5828e-16 m=1
\+89 (Q_NOT 14) capacitor c=2.2914e-16 m=1
\+88 (Q_NOT 13) capacitor c=4.5828e-16 m=1
\+87 (Q_NOT 0) capacitor c=7.76235e-16 m=1
\+86 (Q_NOT MASTER_QNOT) capacitor c=2.2914e-16 m=1
\+85 (Q_NOT Q) capacitor c=4.5828e-16 m=1
\+84 (Q_NOT vdd!) capacitor c=3.2085e-15 m=1
\+83 (Q_NOT MASTER_Q) capacitor c=4.5828e-16 m=1
\+82 (CLK_NOT 27) capacitor c=6.8742e-16 m=1
```

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\+81 (CLK_NOT 26) capacitor c=4.5828e-16 m=1
\+80 (CLK_NOT 20) capacitor c=4.5828e-16 m=1
\+79 (CLK_NOT 19) capacitor c=2.25433e-15 m=1
\+78 (CLK_NOT 16) capacitor c=4.5828e-16 m=1
\+77 (CLK_NOT 15) capacitor c=9.1656e-16 m=1
\+76 (CLK_NOT 14) capacitor c=9.1656e-16 m=1
\+75 (CLK_NOT 13) capacitor c=4.5828e-16 m=1
\+74 (CLK_NOT 12) capacitor c=1.37484e-15 m=1
\+73 (CLK_NOT 0) capacitor c=6.87544e-15 m=1
\+72 (CLK_NOT MASTER_QNOT) capacitor c=1.37484e-15 m=1
\+71 (CLK_NOT Q) capacitor c=6.8742e-16 m=1
\+70 (CLK_NOT vdd!) capacitor c=4.95135e-15 m=1
\+69 (CLK_NOT MASTER_Q) capacitor c=9.1656e-16 m=1
\+68 (CLK_NOT Q_NOT) capacitor c=4.5828e-16 m=1
\+33 (28 27 0 0) ami06N w=1.17e-05 l=6e-07 as=1.053e-11 ad=1.755e-11 \
    ps=1.8e-06 pd=1.47e-05 m=1 region=sat
\+32 (29 Q_NOT 0 0) ami06N w=1.17e-05 l=6e-07 as=1.053e-11 \
    ad=1.755e-11 ps=1.8e-06 pd=1.47e-05 m=1 region=sat
\+31 (0 27 28 0) ami06N w=1.17e-05 l=6e-07 as=1.053e-11 ad=1.053e-11 \
    ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+30 (0 Q_NOT 29 0) ami06N w=1.17e-05 l=6e-07 as=1.053e-11 \
    ad=1.053e-11 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+29 (28 Q Q_NOT 0) ami06N w=1.17e-05 l=6e-07 as=1.053e-11 \
    ad=1.053e-11 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+28 (29 26 Q 0) ami06N w=1.17e-05 l=6e-07 as=1.053e-11 ad=1.053e-11 \
    ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+27 (Q 26 29 0) ami06N w=1.17e-05 l=6e-07 as=1.755e-11 ad=1.053e-11 \
    ps=1.47e-05 pd=1.8e-06 m=1 region=sat
\+26 (Q_NOT Q 28 0) ami06N w=1.17e-05 l=6e-07 as=1.755e-11 \
    ad=1.053e-11 ps=1.47e-05 pd=1.8e-06 m=1 region=sat
\+25 (27 15 25 0) ami06N w=9.6e-06 l=6e-07 as=8.64e-12 ad=1.44e-11 \
    ps=1.8e-06 pd=1.26e-05 m=1 region=sat
\+24 (26 15 30 0) ami06N w=9.6e-06 l=6e-07 as=4.32e-12 ad=1.44e-11 \
    ps=9e-07 pd=1.26e-05 m=1 region=sat
\+23 (25 MASTER_QNOT 0 0) ami06N w=9.6e-06 l=6e-07 as=1.44e-11 \
    ad=8.64e-12 ps=1.26e-05 pd=1.8e-06 m=1 region=sat
\+22 (30 MASTER_Q 0 0) ami06N w=9.6e-06 l=6e-07 as=1.44e-11 \
    ad=4.32e-12 ps=1.26e-05 pd=9e-07 m=1 region=sat
\+21 (0 MASTER_Q 21 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 ad=9e-12 \
    ps=1.8e-06 pd=9e-06 m=1 region=sat
\+20 (0 13 22 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 ad=9e-12 ps=1.8e-06 \
    pd=9e-06 m=1 region=sat
\+19 (21 19 23 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 ad=5.4e-12 \
    ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+18 (22 20 24 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 ad=5.4e-12 \
    ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+17 (23 12 MASTER_QNOT 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 \
    ad=5.4e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+16 (24 MASTER_QNOT MASTER_Q 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 \
    ad=5.4e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+15 (MASTER_QNOT 12 23 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 \
    ad=5.4e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+14 (MASTER_Q MASTER_QNOT 24 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 \
    ad=5.4e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+13 (23 19 21 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 ad=5.4e-12 \
    ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+12 (24 20 22 0) ami06N w=6e-06 l=6e-07 as=5.4e-12 ad=5.4e-12 \
    ps=1.8e-06 pd=1.8e-06 m=1 region=sat
\+11 (21 MASTER_Q 0 0) ami06N w=6e-06 l=6e-07 as=9e-12 ad=5.4e-12 \
    ps=9e-06 pd=1.8e-06 m=1 region=sat
\+10 (22 13 0 0) ami06N w=6e-06 l=6e-07 as=9e-12 ad=5.4e-12 ps=9e-06 \
    pd=1.8e-06 m=1 region=sat
\+9 (19 CLK_NOT 17 0) ami06N w=4.2e-06 l=6e-07 as=3.78e-12 ad=6.3e-12 \
    ps=1.8e-06 pd=7.2e-06 m=1 region=sat
\+8 (20 16 18 0) ami06N w=4.2e-06 l=6e-07 as=3.78e-12 ad=6.3e-12 \
    ps=1.8e-06 pd=7.2e-06 m=1 region=sat
\+7 (17 14 0 0) ami06N w=4.2e-06 l=6e-07 as=6.3e-12 ad=3.78e-12 \
    ps=7.2e-06 pd=1.8e-06 m=1 region=sat
\+6 (18 CLK_NOT 0 0) ami06N w=4.2e-06 l=6e-07 as=6.3e-12 ad=3.78e-12 \
    ps=7.2e-06 pd=1.8e-06 m=1 region=sat
\+5 (16 14 0 0) ami06N w=1.5e-06 l=6e-07 as=2.25e-12 ad=2.25e-12 \
    ps=4.5e-06 pd=4.5e-06 m=1 region=sat
\+3 (14 D 0 0) ami06N w=1.5e-06 l=6e-07 as=2.25e-12 ad=2.25e-12 \
    ps=4.5e-06 pd=4.5e-06 m=1 region=sat
```

```
    \+4 (CLK_NOT CLK 0 0) ami06N w=3e-06 l=6e-07 as=4.5e-12 ad=4.5e-12 \
        ps=6e-06 pd=6e-06 m=1 region=sat
    \+2 (15 CLK_NOT 0 0) ami06N w=3.9e-06 l=6e-07 as=5.85e-12 ad=5.85e-12 \
        ps=6.9e-06 pd=6.9e-06 m=1 region=sat
    \+1 (12 PRESET 0 0) ami06N w=2.1e-06 l=6e-07 as=3.15e-12 ad=3.15e-12 \
        ps=5.1e-06 pd=5.1e-06 m=1 region=sat
    \+0 (13 CLEAR 0 0) ami06N w=2.1e-06 l=6e-07 as=3.15e-12 ad=3.15e-12 \
        ps=5.1e-06 pd=5.1e-06 m=1 region=sat
    \+59 (vdd! 15 27 vdd!) ami06P w=9.6e-06 l=6e-07 as=8.64e-12 \
        ad=1.44e-11 ps=1.8e-06 pd=1.26e-05 m=1 region=sat
    \+58 (vdd! 15 26 vdd!) ami06P w=9.6e-06 l=6e-07 as=8.64e-12 \
        ad=1.44e-11 ps=1.8e-06 pd=1.26e-05 m=1 region=sat
    \+57 (27 MASTER_QNOT vdd! vdd!) ami06P w=9.6e-06 l=6e-07 as=1.44e-11 \
        ad=8.64e-12 ps=1.26e-05 pd=1.8e-06 m=1 region=sat
    \+56 (26 MASTER_Q vdd! vdd!) ami06P w=9.6e-06 l=6e-07 as=1.44e-11 \
        ad=8.64e-12 ps=1.26e-05 pd=1.8e-06 m=1 region=sat
    \+55 (vdd! MASTER_Q MASTER_QNOT vdd!) ami06P w=4.05e-06 l=6e-07 \
        as=3.645e-12 ad=6.075e-12 ps=1.8e-06 pd=7.05e-06 m=1 region=sat
    \+54 (vdd! 13 MASTER_Q vdd!) ami06P w=4.05e-06 l=6e-07 as=3.645e-12 \
        ad=6.075e-12 ps=1.8e-06 pd=7.05e-06 m=1 region=sat
    \+53 (MASTER_QNOT 19 vdd! vdd!) ami06P w=4.05e-06 l=6e-07 as=3.645e-12 \
        ad=3.645e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+52 (MASTER_Q 20 vdd! vdd!) ami06P w=4.05e-06 l=6e-07 as=3.645e-12 \
        ad=3.645e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+51 (vdd! MASTER_QNOT MASTER_Q vdd!) ami06P w=4.05e-06 l=6e-07 \
        as=3.645e-12 ad=3.645e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+50 (vdd! 12 MASTER_QNOT vdd!) ami06P w=4.05e-06 l=6e-07 as=3.645e-12 \
        ad=3.645e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+49 (MASTER_QNOT 12 vdd! vdd!) ami06P w=4.05e-06 l=6e-07 as=3.645e-12 \
        ad=3.645e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+48 (MASTER_Q MASTER_QNOT vdd! vdd!) ami06P w=4.05e-06 l=6e-07 \
        as=3.645e-12 ad=3.645e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+47 (vdd! 19 MASTER_QNOT vdd!) ami06P w=4.05e-06 l=6e-07 as=3.645e-12 \
        ad=3.645e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+46 (vdd! 20 MASTER_Q vdd!) ami06P w=4.05e-06 l=6e-07 as=3.645e-12 \
        ad=3.645e-12 ps=1.8e-06 pd=1.8e-06 m=1 region=sat
    \+45 (MASTER_QNOT MASTER_Q vdd! vdd!) ami06P w=4.05e-06 l=6e-07 \
        as=6.075e-12 ad=3.645e-12 ps=7.05e-06 pd=1.8e-06 m=1 region=sat
    \+44 (MASTER_Q 13 vdd! vdd!) ami06P w=4.05e-06 l=6e-07 as=6.075e-12 \
        ad=3.645e-12 ps=7.05e-06 pd=1.8e-06 m=1 region=sat
    \+43 (vdd! CLK_NOT 19 vdd!) ami06P w=4.2e-06 l=6e-07 as=3.78e-12 \
        ad=6.3e-12 ps=1.8e-06 pd=7.2e-06 m=1 region=sat
    \+42 (vdd! 16 20 vdd!) ami06P w=4.2e-06 l=6e-07 as=3.78e-12 ad=6.3e-12 \
        ps=1.8e-06 pd=7.2e-06 m=1 region=sat
    \+41 (19 14 vdd! vdd!) ami06P w=4.2e-06 l=6e-07 as=6.3e-12 ad=3.78e-12 \
        ps=7.2e-06 pd=1.8e-06 m=1 region=sat
    \+40 (20 CLK_NOT vdd! vdd!) ami06P w=4.2e-06 l=6e-07 as=6.3e-12 \
        ad=3.78e-12 ps=7.2e-06 pd=1.8e-06 m=1 region=sat
    \+35 (12 PRESET vdd! vdd!) ami06P w=4.2e-06 l=6e-07 as=6.3e-12 \
        ad=6.3e-12 ps=7.2e-06 pd=7.2e-06 m=1 region=sat
    \+34 (13 CLEAR vdd! vdd!) ami06P w=4.2e-06 l=6e-07 as=6.3e-12 \
        ad=6.3e-12 ps=7.2e-06 pd=7.2e-06 m=1 region=sat
    \+38 (16 14 vdd! vdd!) ami06P w=3e-06 l=6e-07 as=4.5e-12 ad=4.5e-12 \
        ps=6e-06 pd=6e-06 m=1 region=sat
    \+37 (14 D vdd! vdd!) ami06P w=3e-06 l=6e-07 as=4.5e-12 ad=4.5e-12 \
        ps=6e-06 pd=6e-06 m=1 region=sat
    \+39 (CLK_NOT CLK vdd! vdd!) ami06P w=6e-06 l=6e-07 as=9e-12 ad=9e-12 \
        ps=9e-06 pd=9e-06 m=1 region=sat
    \+36 (15 CLK_NOT vdd! vdd!) ami06P w=7.8e-06 l=6e-07 as=1.17e-11 \
        ad=1.17e-11 ps=1.08e-05 pd=1.08e-05 m=1 region=sat
ends Design
// End of subcircuit definition.

// Library name: Project
// Cell name: sim_Design
// View name: schematic
// Inherited view list: spectre cmos_sch cmos.sch schematic veriloga ahdl
// pspice dspf
I4 (CLEAR CLK D PRESET Q Q_NOT CLK_NOT MASTER_Q MASTER_QNOT) Design
C1 (Q 0) capacitor c=228.8368978f m=1
C0 (Q_NOT 0) capacitor c=228.8368978f m=1
include "./_graphical_stimuli.scs"
simulatorOptions options psfversion="1.4.0" reltol=1e-3 vabstol=1e-6 \
    iabstol=1e-12 temp=27 tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 \
```

```
    maxnotes=5 maxwarns=5 digits=5 cols=80 pivrel=1e-3 \
    sensfile="../psf/sens.output" checklimitdest=psf
tran tran stop=24n write="spectre.ic" writefinal="spectre.fc" \
    annotate=status maxiters=5
finalTimeOP info what=oppoint where=rawfile
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
save CLK D MASTER_Q MASTER_QNOT CLK_NOT Q_NOT Q Q CLK_NOT MASTER_Q D
saveOptions options save=allpub
```

APPENDIX J
LAYOUT VERSUS SCHEMATIC (LVS) CHECKS

A. Stage U/V: Inverter, LVS

```
@(#)$CDS: LVS version 6.1.8-64b 05/03/2022 19:50 (cpgbld01) $

Command line: /opt/cadence/installs/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/shahkr85/cadence/LVS -l -s -t /hom
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/shahkr85/cadence/LVS/layout/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos

    Net-list summary for /home/shahkr85/cadence/LVS/schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos


    Terminal correspondence points
    N0        N0        gnd!
    N3        N4        in
    N2        N5        out
    N1        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 2       2
        total                  2       2

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 4       4
        total                  4       4

                               terminals
        un-matched             0       0
        matched but
        different type         0       0
        total                  4       4


Probe files from /home/shahkr85/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
```

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/shahkr85/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

B. Stage W: NAND2, LVS

```
@(#)$CDS: LVS version 6.1.8-64b 05/03/2022 19:50 (cpgbld01) $

Command line: /opt/cadence/installs/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/shahkr85/cadence/LVS -l -s -t /hom
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/shahkr85/cadence/LVS/layout/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos

    Net-list summary for /home/shahkr85/cadence/LVS/schematic/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos


    Terminal correspondence points
    N3          N2          A
    N2          N3          B
    N1          N0          gnd!
    N5          N4          out
    N4          N1          vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                             layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                                  nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  6       6
        total                   6       6

                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   5       5


Probe files from /home/shahkr85/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
```

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/shahkr85/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

C. Stage X: NAND3, LVS

```
@(#)$CDS: LVS version 6.1.8-64b 05/03/2022 19:50 (cpgbld01) $

Command line: /opt/cadence/installs/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/shahkr85/cadence/LVS -l -s -t /hom
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/shahkr85/cadence/LVS/layout/netlist
       count
        8               nets
        6               terminals
        6               pmos
        6               nmos

    Net-list summary for /home/shahkr85/cadence/LVS/schematic/netlist
       count
        8               nets
        6               terminals
        6               pmos
        6               nmos


    Terminal correspondence points
    N5        N2        A
    N4        N3        B
    N3        N8        C
    N2        N0        gnd!
    N7        N4        out
    N6        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 12      12
        total                  12      12

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 8       8
        total                  8       8

                               terminals
        un-matched             0       0
        matched but
        different type         0       0
        total                  6       6


Probe files from /home/shahkr85/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
```

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/shahkr85/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

D. Stage Y: NAND2, LVS

```
@(#)$CDS: LVS version 6.1.8-64b 05/03/2022 19:50 (cpgbld01) $

Command line: /opt/cadence/installs/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/shahkr85/cadence/LVS -l -s -t /hom
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/shahkr85/cadence/LVS/layout/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos

    Net-list summary for /home/shahkr85/cadence/LVS/schematic/netlist
       count
        6               nets
        5               terminals
        2               pmos
        2               nmos


    Terminal correspondence points
    N3          N2          A
    N2          N3          B
    N1          N0          gnd!
    N5          N4          out
    N4          N1          vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                             layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                                  nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  6       6
        total                   6       6

                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   5       5


Probe files from /home/shahkr85/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
```

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/shahkr85/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

E. Stage Z: NAND2, LVS

```
@(#)$CDS: LVS version 6.1.8-64b 05/03/2022 19:50 (cpgbld01) $

Command line: /opt/cadence/installs/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/shahkr85/cadence/LVS -l -s -t /hom
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/shahkr85/cadence/LVS/layout/netlist
       count
        6               nets
        5               terminals
        4               pmos
        4               nmos

    Net-list summary for /home/shahkr85/cadence/LVS/schematic/netlist
       count
        6               nets
        5               terminals
        4               pmos
        4               nmos


    Terminal correspondence points
    N3          N2          A
    N2          N3          B
    N1          N0          gnd!
    N5          N4          out
    N4          N1          vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                             layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  8       8
        total                   8       8

                                  nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  6       6
        total                   6       6

                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   5       5


Probe files from /home/shahkr85/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
```

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/shahkr85/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

F. PRESET/CLEAR: Inverter, LVS

```
@(#)$CDS: LVS version 6.1.8-64b 05/03/2022 19:50 (cpgbld01) $

Command line: /opt/cadence/installs/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/shahkr85/cadence/LVS -l -s -t /hom
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/shahkr85/cadence/LVS/layout/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos

    Net-list summary for /home/shahkr85/cadence/LVS/schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos


    Terminal correspondence points
    N0        N0        gnd!
    N3        N4        in
    N2        N5        out
    N1        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 2       2
        total                  2       2

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 4       4
        total                  4       4

                               terminals
        un-matched             0       0
        matched but
        different type         0       0
        total                  4       4


Probe files from /home/shahkr85/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:
```

prunedev.out:

audit.out:

Probe files from /home/shahkr85/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

G. Clock Master: Inverter, LVS

```
@(#)$CDS: LVS version 6.1.8-64b 05/03/2022 19:50 (cpgbld01) $

Command line: /opt/cadence/installs/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/shahkr85/cadence/LVS -l -s -t /hom
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/shahkr85/cadence/LVS/layout/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos

    Net-list summary for /home/shahkr85/cadence/LVS/schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos


    Terminal correspondence points
    N0        N0        gnd!
    N3        N4        in
    N2        N5        out
    N1        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 2       2
        total                  2       2

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 4       4
        total                  4       4

                               terminals
        un-matched             0       0
        matched but
        different type         0       0
        total                  4       4


Probe files from /home/shahkr85/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:
```

prunedev.out:

audit.out:

Probe files from /home/shahkr85/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

H. Clock Slave: Inverter, LVS

```
@(#)$CDS: LVS version 6.1.8-64b 05/03/2022 19:50 (cpgbld01) $

Command line: /opt/cadence/installs/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/shahkr85/cadence/LVS -l -s -t /hom
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/shahkr85/cadence/LVS/layout/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos

    Net-list summary for /home/shahkr85/cadence/LVS/schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos


    Terminal correspondence points
    N0        N0        gnd!
    N3        N4        in
    N2        N5        out
    N1        N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 2       2
        total                  2       2

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 4       4
        total                  4       4

                               terminals
        un-matched             0       0
        matched but
        different type         0       0
        total                  4       4


Probe files from /home/shahkr85/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:
```

prunedev.out:

audit.out:

Probe files from /home/shahkr85/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

I. Snap-Together Layout, LVS

```
@(#)$CDS: LVS version 6.1.8-64b 05/03/2022 19:50 (cpgbld01) $

Command line: /opt/cadence/installs/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/shahkr85/cadence/LVS -l -s -t /hom
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/shahkr85/cadence/LVS/layout/netlist
       count
        30              nets
        11              terminals
        34              pmos
        34              nmos

    Net-list summary for /home/shahkr85/cadence/LVS/schematic/netlist
       count
        30              nets
        11              terminals
        34              pmos
        34              nmos


    Terminal correspondence points
    N27       N5        CLEAR
    N22       N2        CLK
    N28       N7        CLK_NOT
    N23       N3        D
    N25       N20       MASTER_Q
    N20       N21       MASTER_QNOT
    N29       N4        PRESET
    N21       N6        Q
    N26       N19       Q_NOT
    N19       N0        gnd!
    N24       N1        vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 68      68
        total                  68      68

                                 nets
        un-matched             0       0
        merged                 0       0
        pruned                 0       0
        active                 30      30
        total                  30      30

                               terminals
        un-matched             0       0
        matched but
        different type         0       0
        total                  11      11


Probe files from /home/shahkr85/cadence/LVS/schematic

devbad.out:
```

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/shahkr85/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out: